

Compal Confidential

STORM2 M/B Schematic

LA-E291P

Rev: 0.3_B

2016.09.01

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	COVER PAGE
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				Date	Thursday, September 01, 2016
				Sheet	1 of 75
				Rev	0.3

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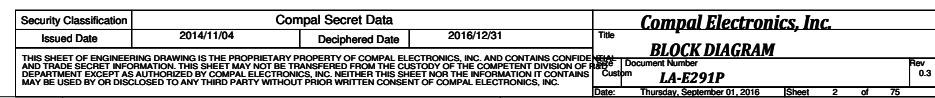
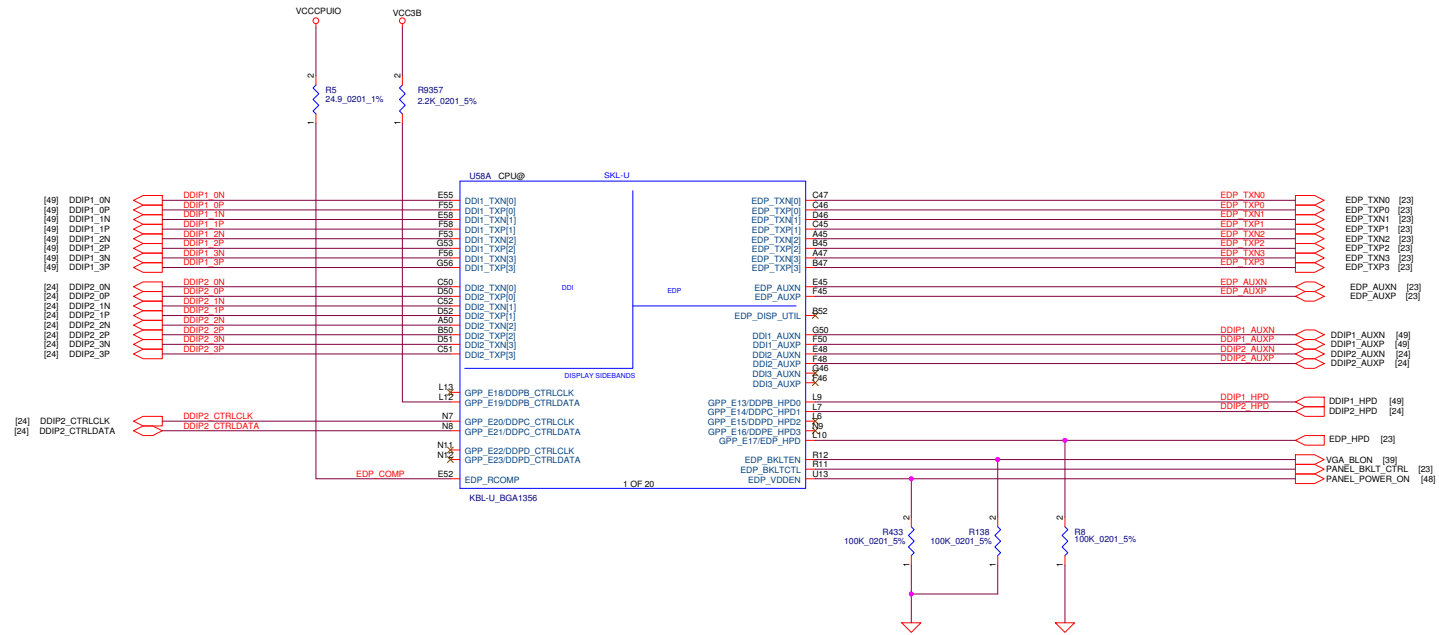


TABLE : Functional Strap

DDPB_CTRLDATA	
HIGH	Port B is detected.
LOW	Port B is not detected.

DDPC_CTRLDATA	
HIGH	Port C is detected.
LOW	Port C is not detected.

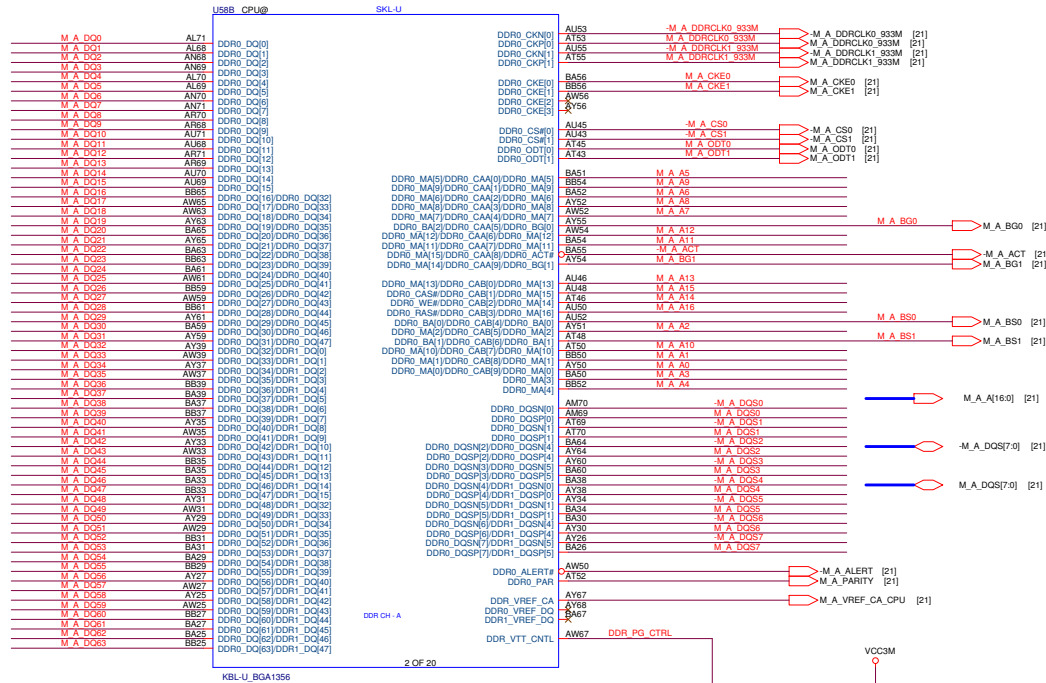


[21] M_A_DQ[63:0]

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
Block 2	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 4	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
Block 6	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 0	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
Block 2	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 4	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
Block 6	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]

LOGIC



TABLE

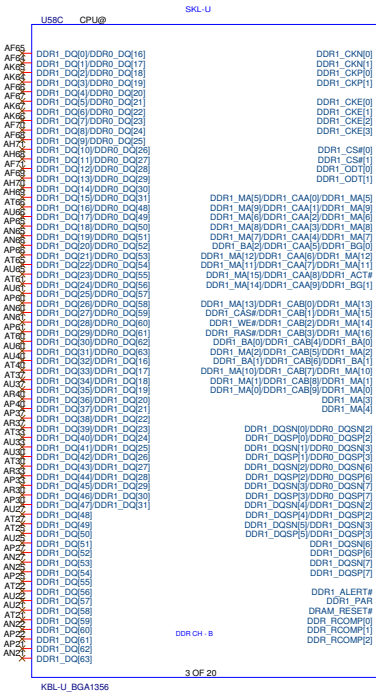
	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]

LOGIC

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AT22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



TABLE

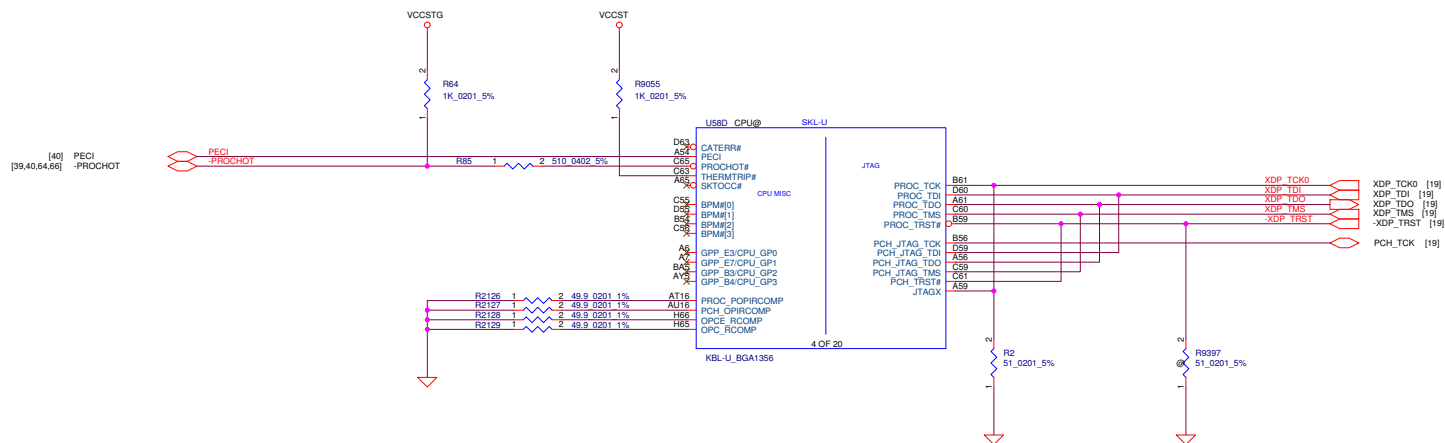
	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC



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SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

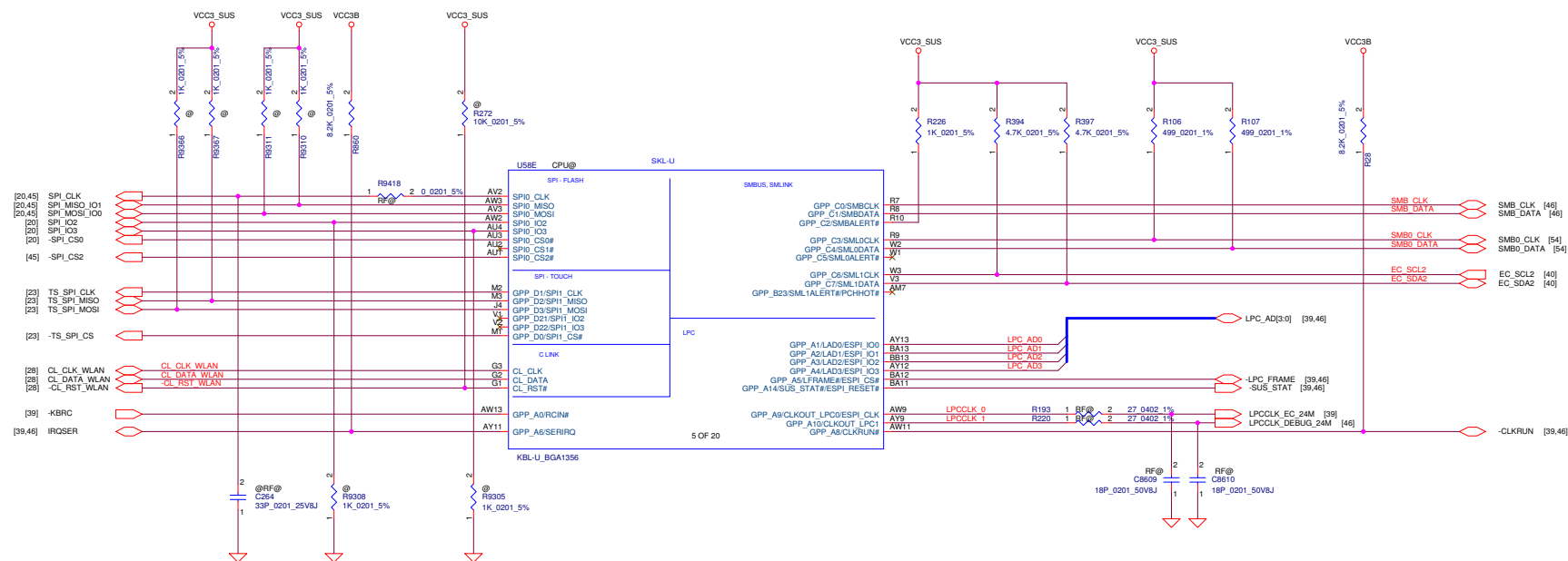
SPI0_MISO (JTAG ODT Diable)	
HIGH	Enabled (Default)
LOW	Disabled

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

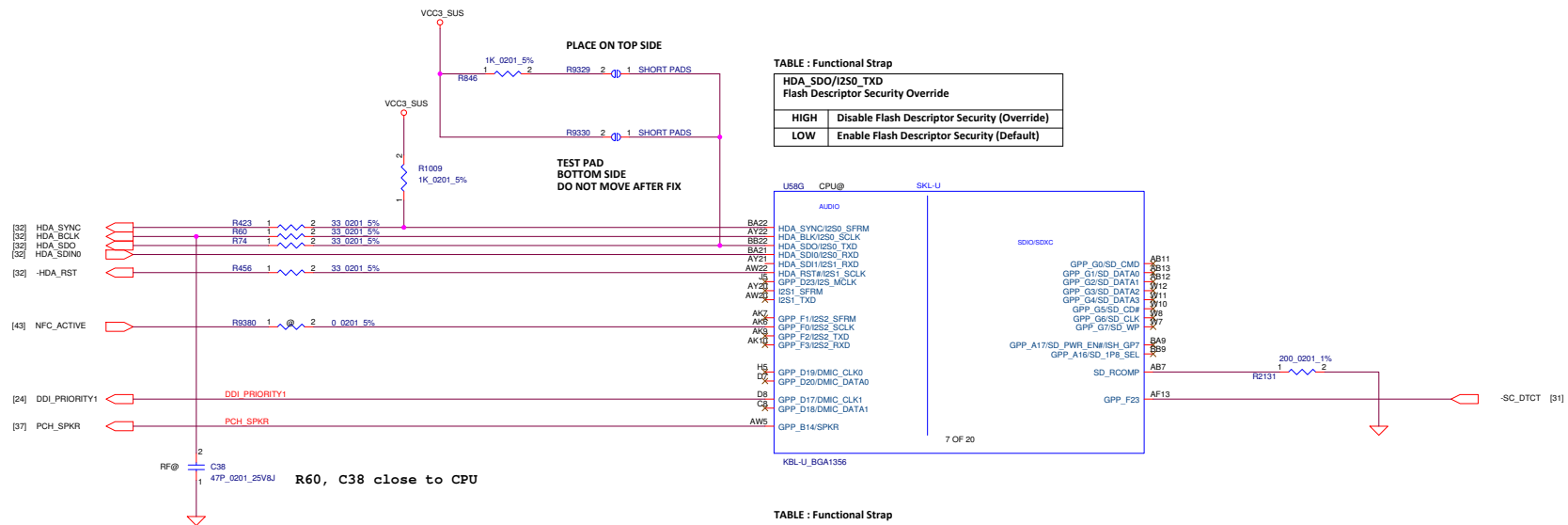
← LOGIC

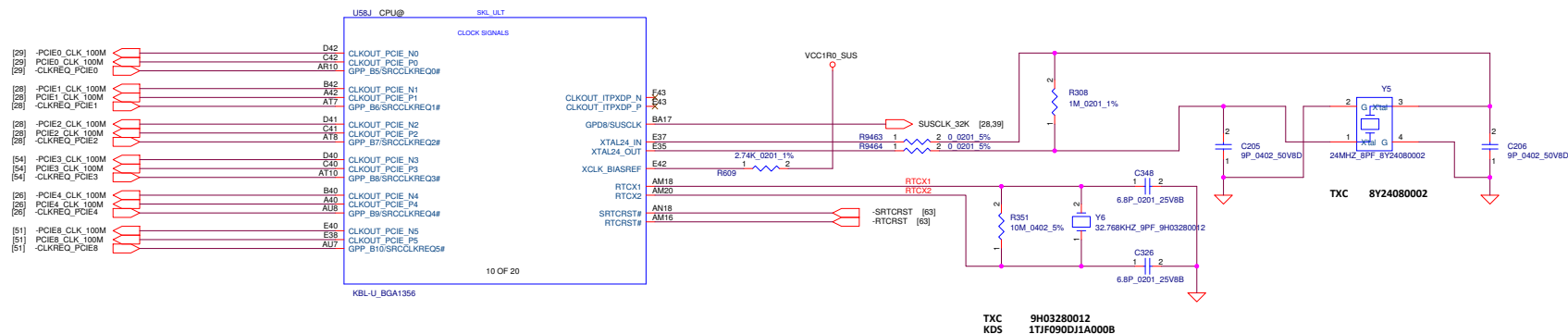


SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

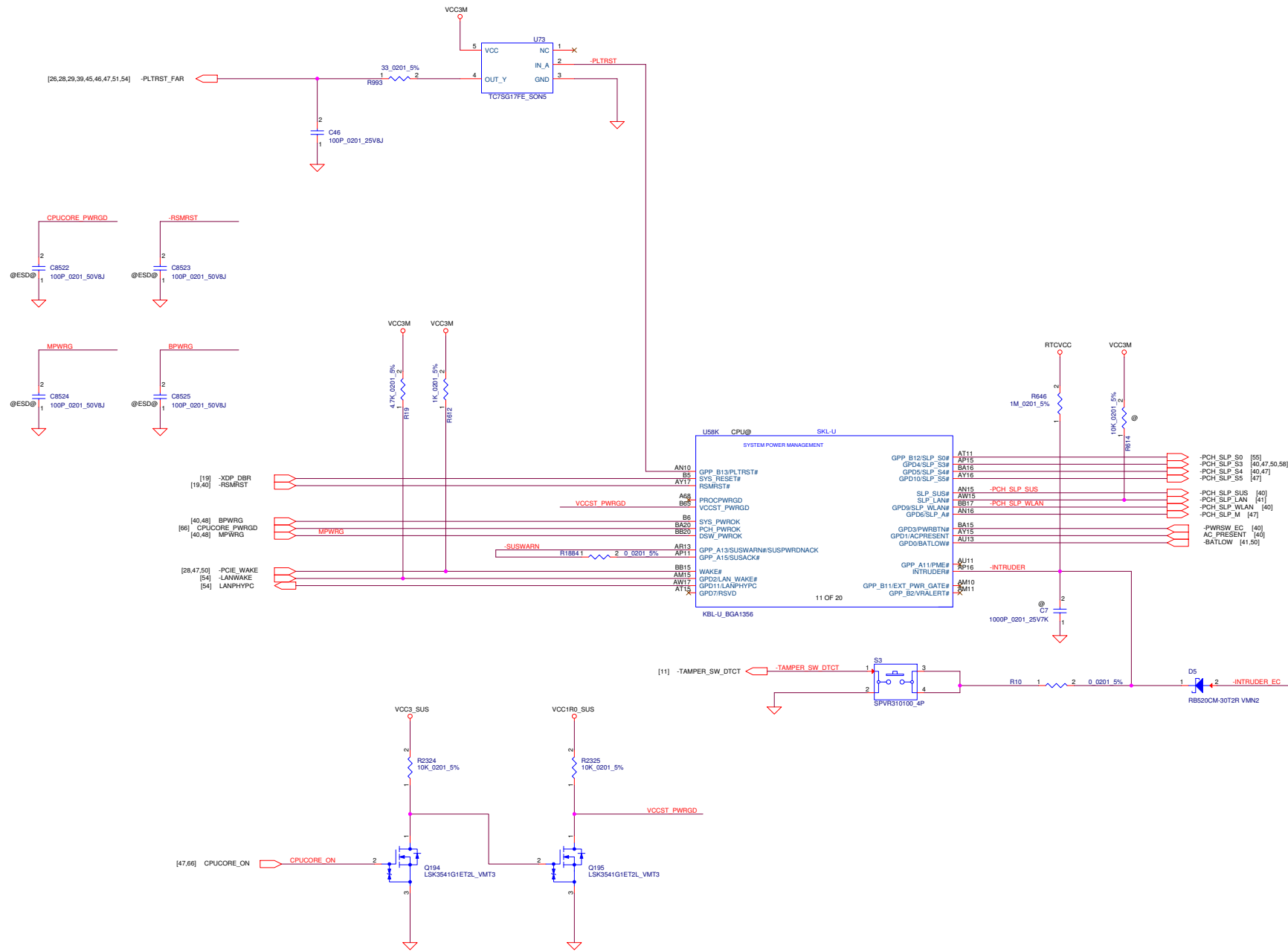
SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc. CPU(i16) : LPC/SPI/SMBUS/C-LINK Document Number: LA-E291P Date: July 29, September 01, 2016 Sheet 7 of 76
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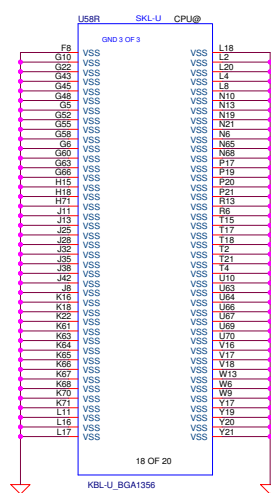
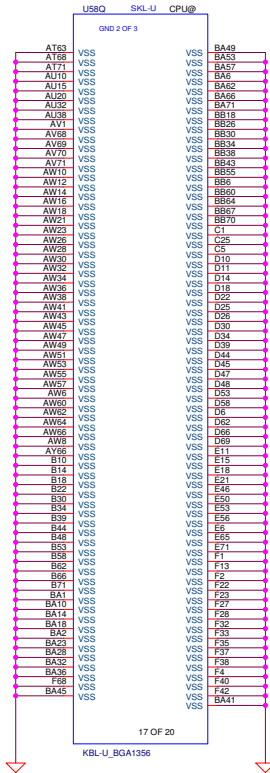
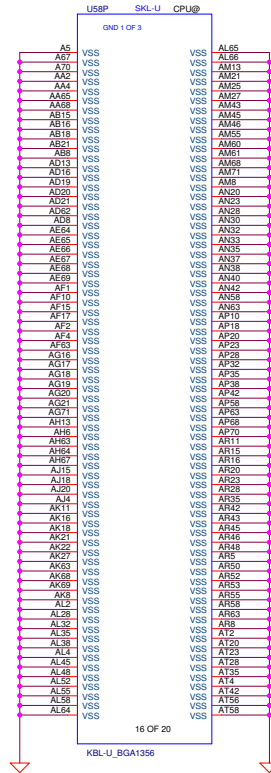




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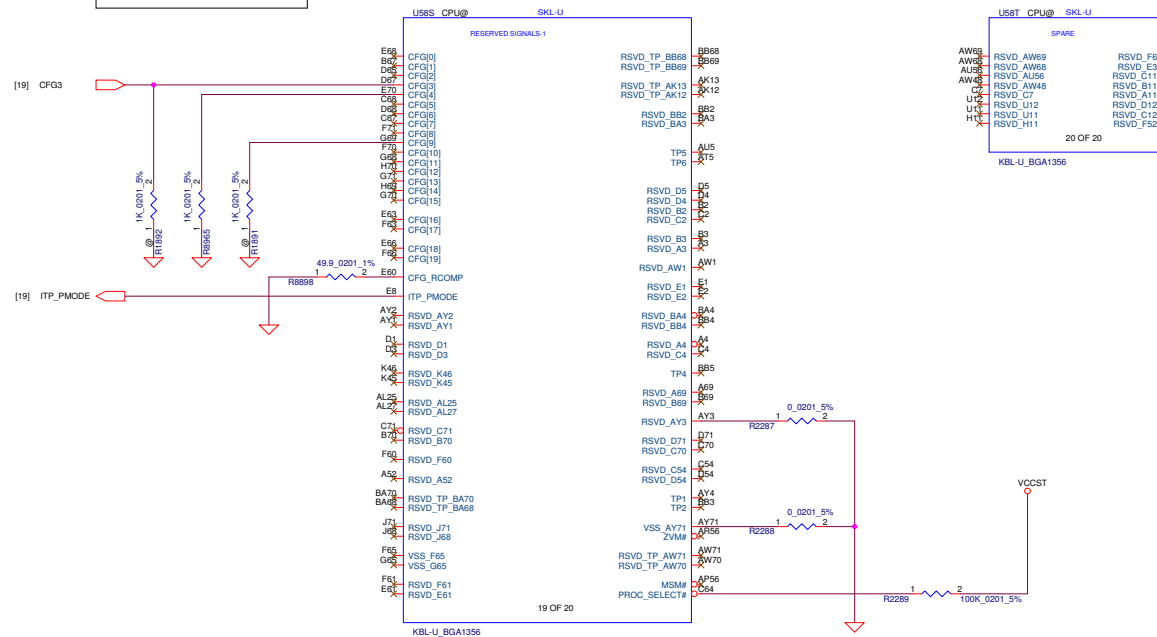
TABLE

CFG0 : Stall Reset Sequence
after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG3 : MSR Privacy Bit Feature
1 : MSR (C80h) bit[0] setting
0 : MSR (C80h) bit[0] overridden

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled



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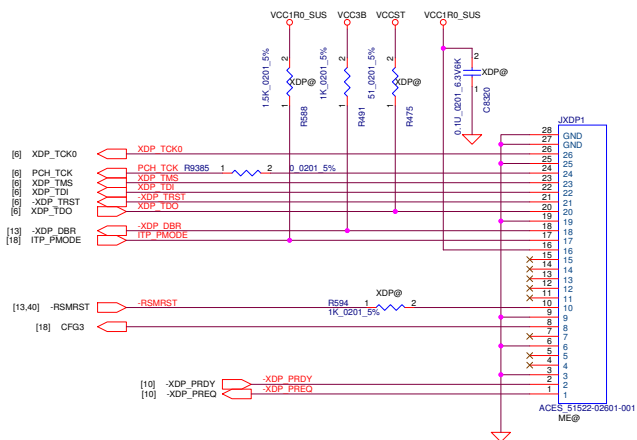
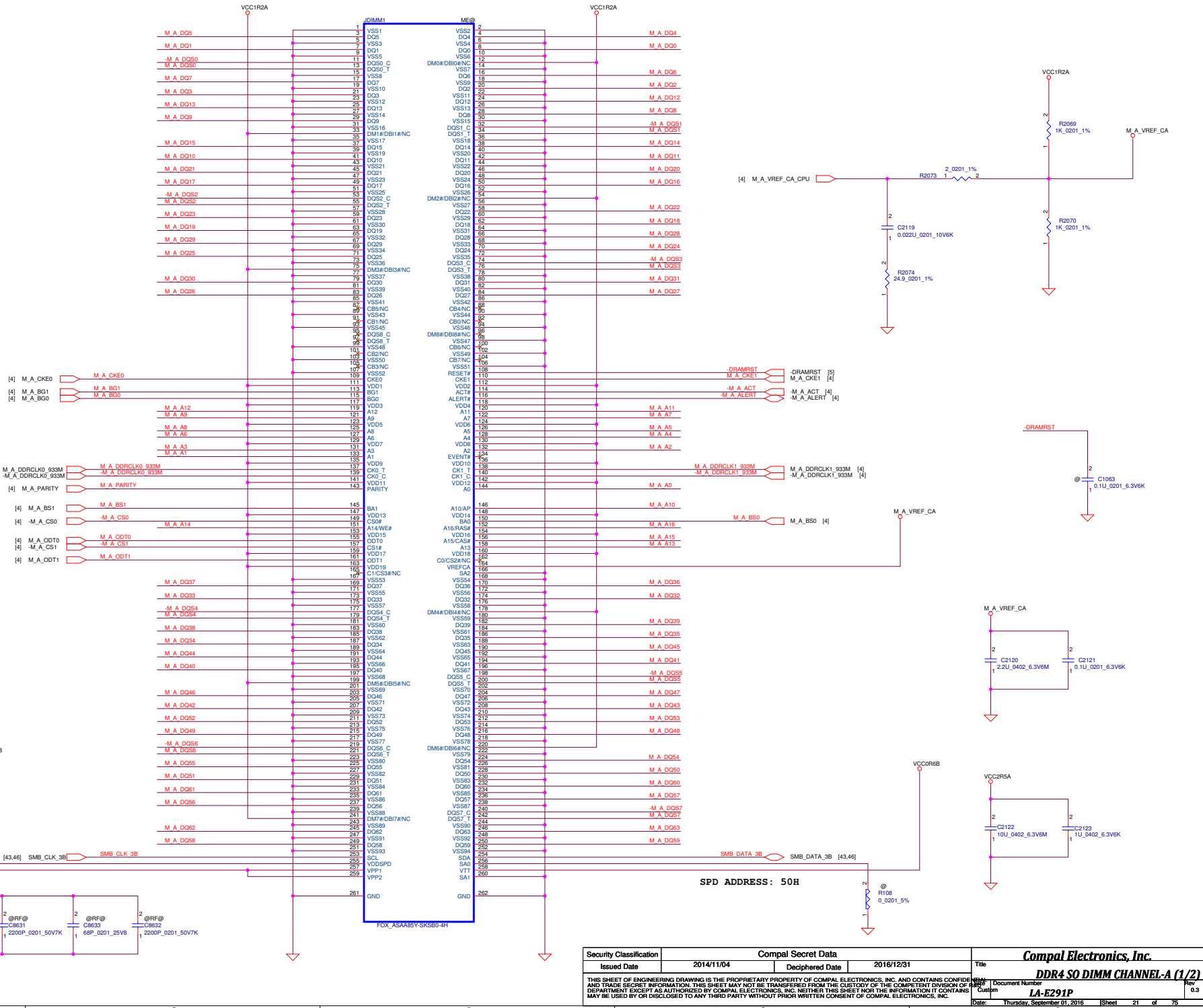
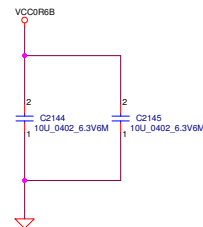
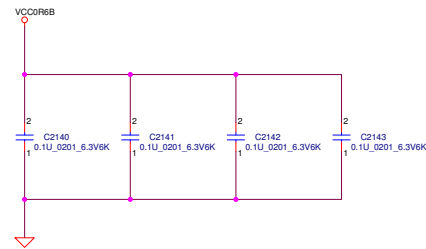
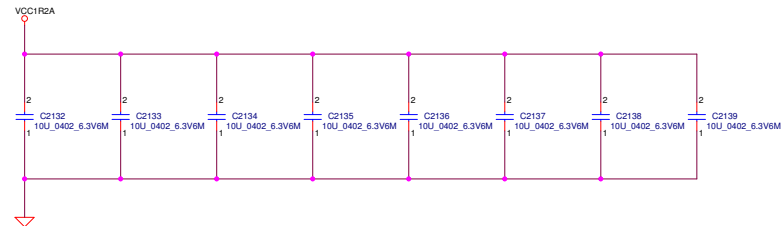
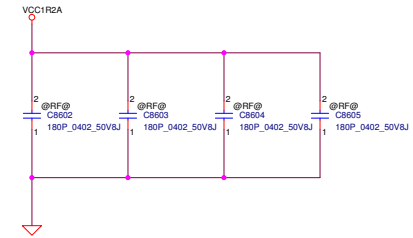
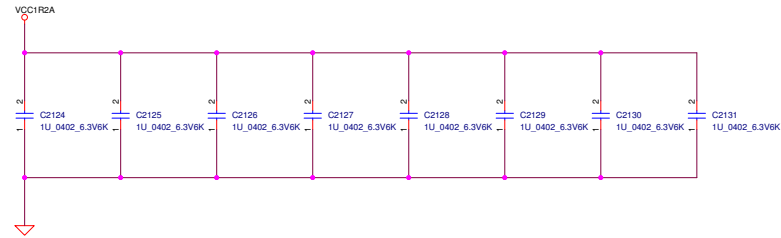


TABLE			
Logic	Ref Des	Merged	DCI 2.0
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Page 18	R1982	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
	R588	ASM	NO_ASM
	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM



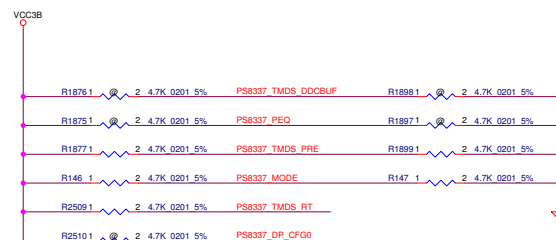


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	DDR4 SO DIMM CHANNEL-A (2/2)
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**Compal Electronics, Inc.**

LCD/LID/MIC/CAMERA

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SW (DDI_PRIORITY1)
<p>L DP Port has higher priority when both ports are plugged</p> <p>H TMDS Port has higher priority when both ports are plugged</p>

TMD5 DDCBUF (INT PD)	R1876	R1898	
DDC Active Buffer	ASM	NO_ASM	
DDC Pass Through w/ PU	ASM	ASM	
DDC Pass Through w/o PU	NO_ASM	NO_ASM	← LOGIC

PEQ (INT PD)	R1875	R1897	
HEQ 15dB	ASM	NO_ASM	
LLEQ 5dB	ASM	ASM	
LEQ 12dB	NO_ASM	NO_ASM	← LOGIC

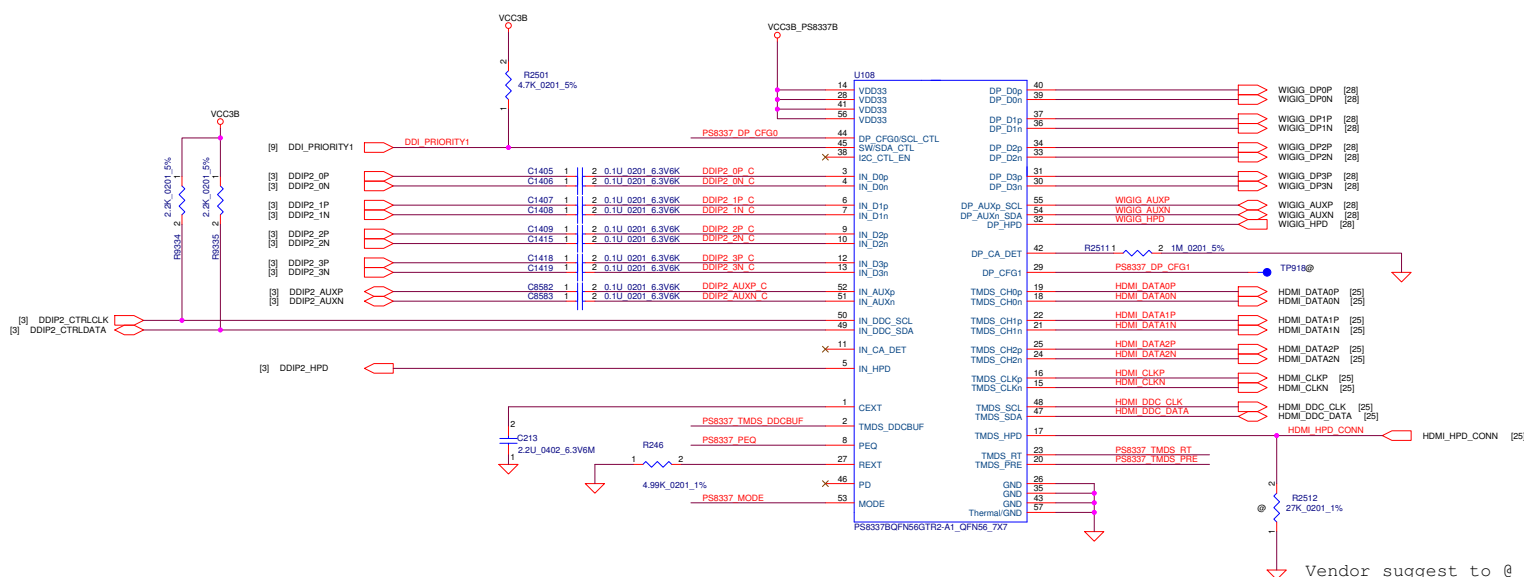
TMD5 PRE (INT PD)	R1877	R1899
1.5dB	ASM	NO_ASM
3.0dB	ASM	ASM
0dB	NO_ASM	NO_ASM

← LOGIC

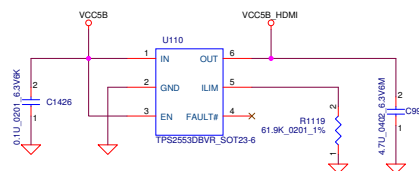
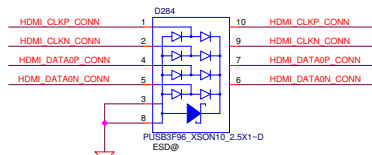
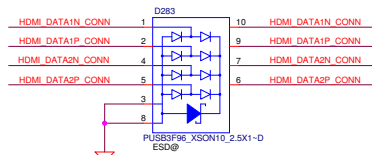
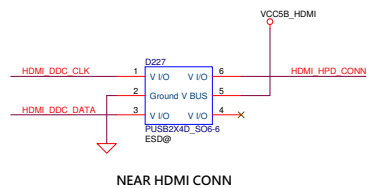
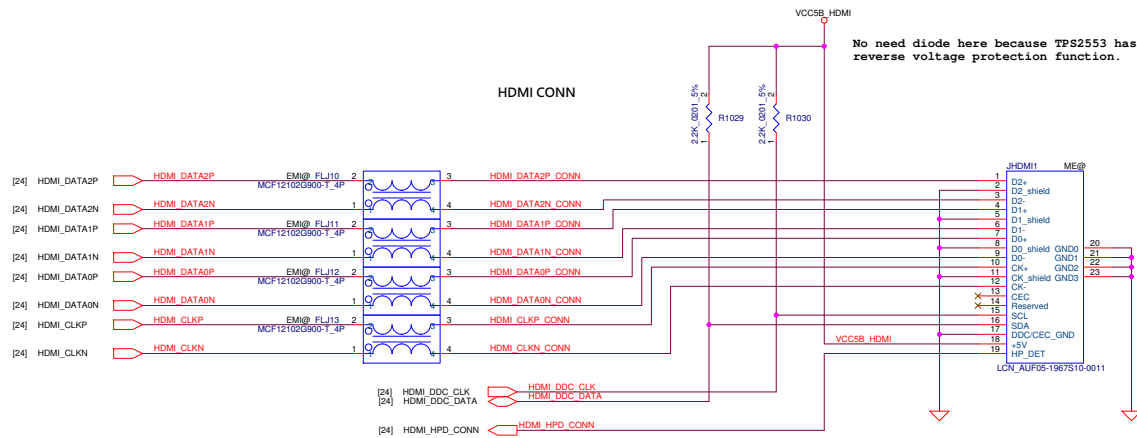
MODE (INT PD)	R146	R147
Auto HDMI ID disable	ASM	NO_ASM
Auto HDMI ID enable	ASM	ASM
Control HDMI ID disable	NO_ASM	NO_ASM

← LOGIC

TMDS RT (INT PD)	R2509
OD w/ termination	ASM
OD	NO_ASM

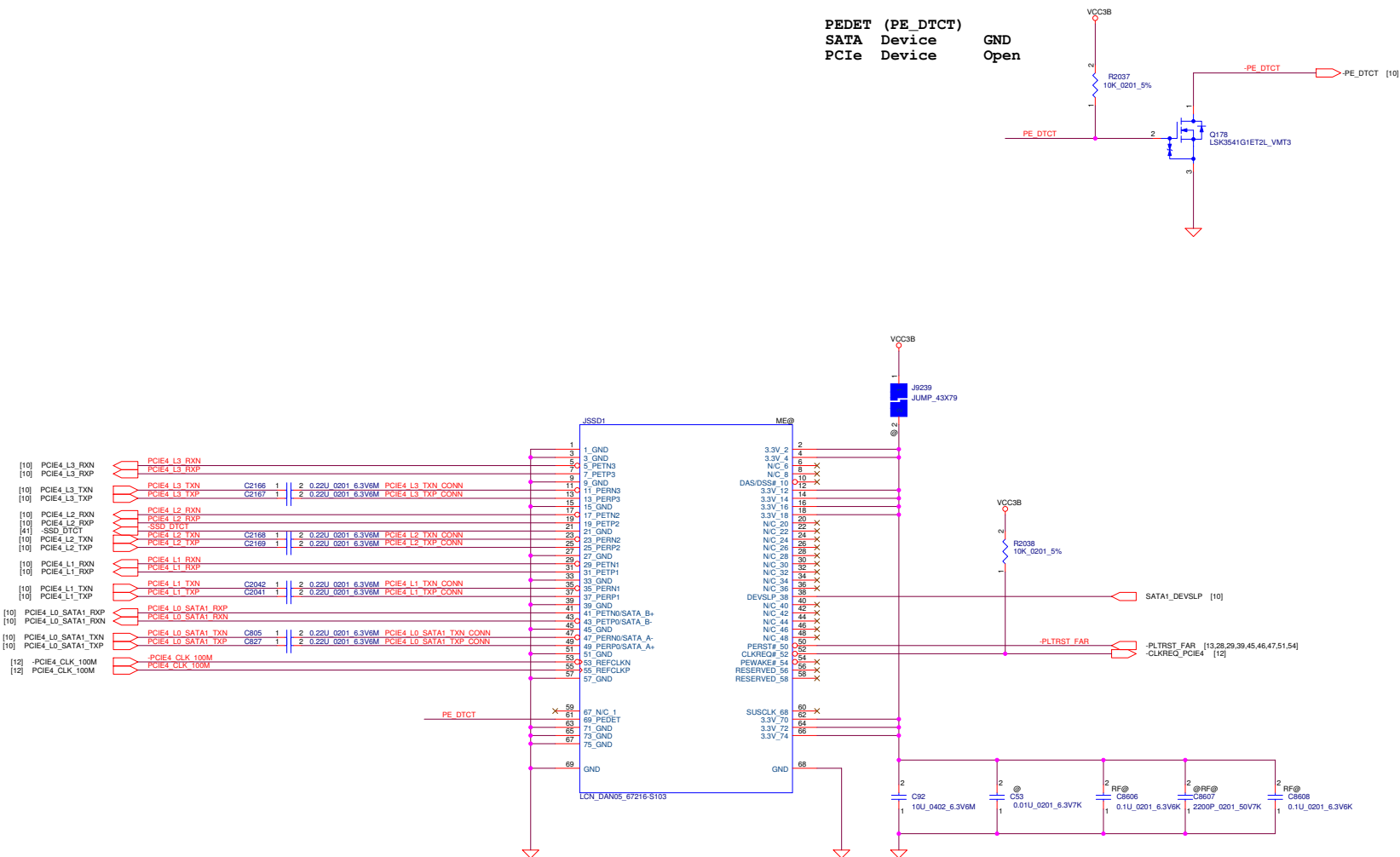


Vendor suggest to @



Current Limit Target : 400mA
Requirement : 300mA
HDMI Spec : 50mA - 500mA

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Issued Date	2014/11/04	Deciphered Date	2016/12/31	HDMI CONNECTOR	
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	M.2 SSD SLOT
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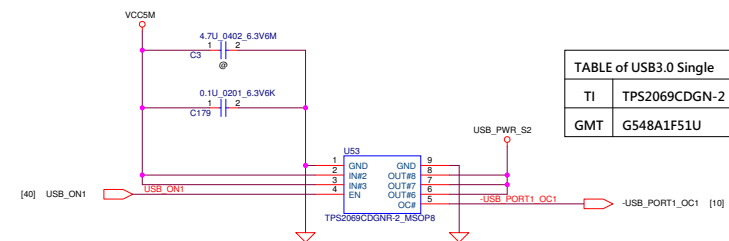
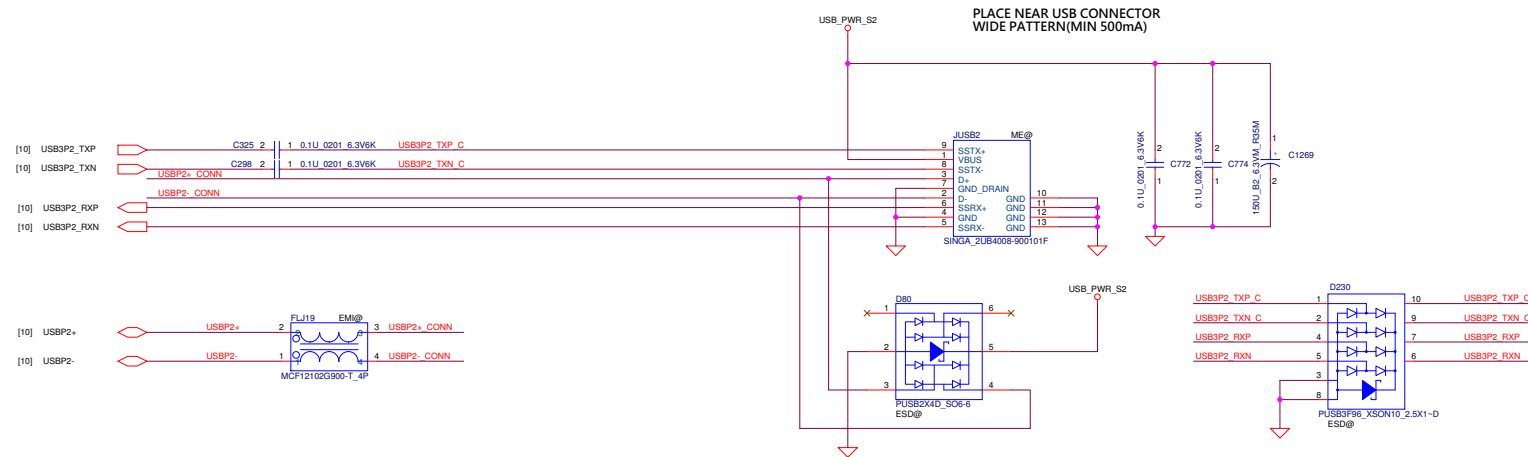
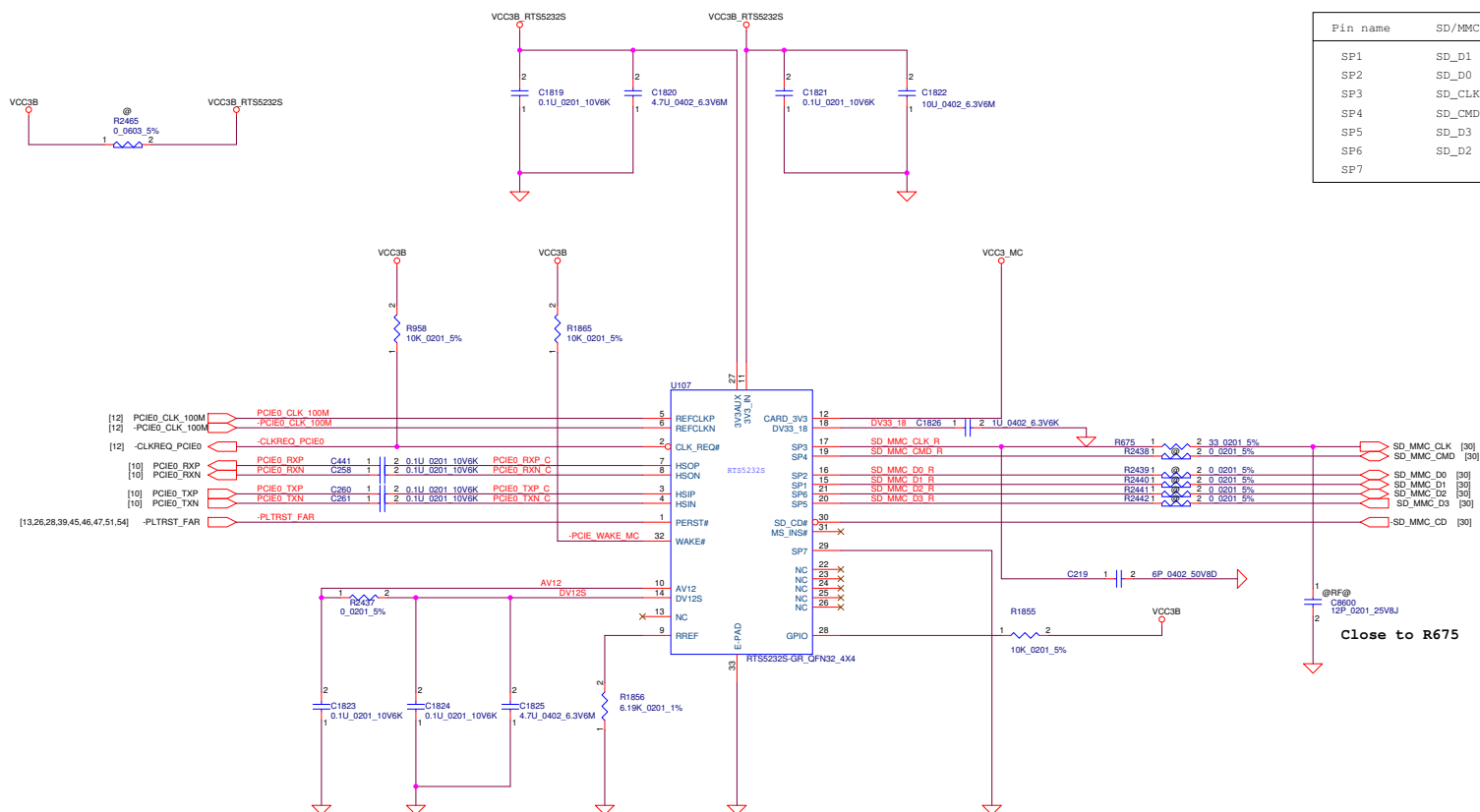
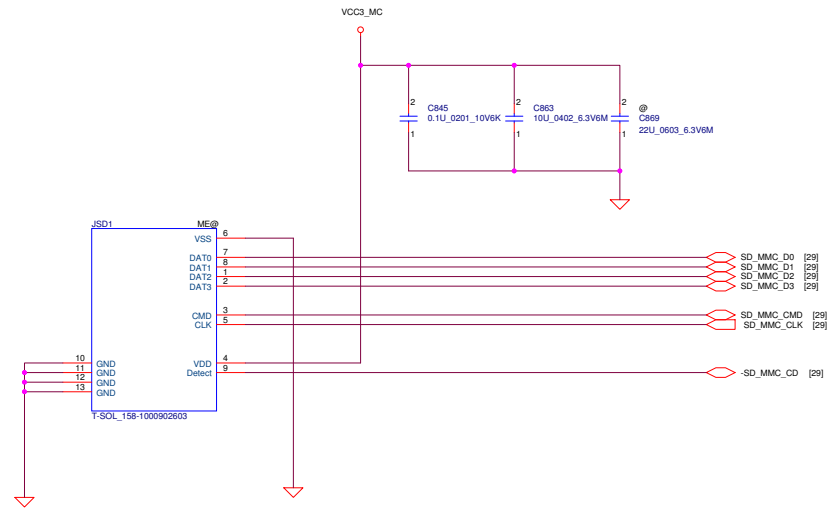


TABLE of USB3.0 Single	
TI	TPS2069CDGN-2
GMT	G548A1F51U

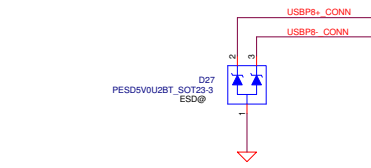
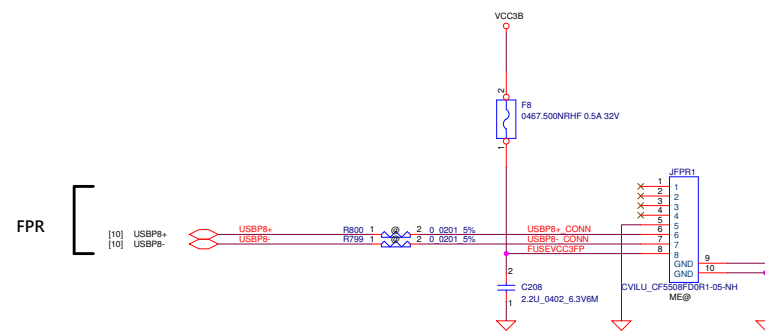
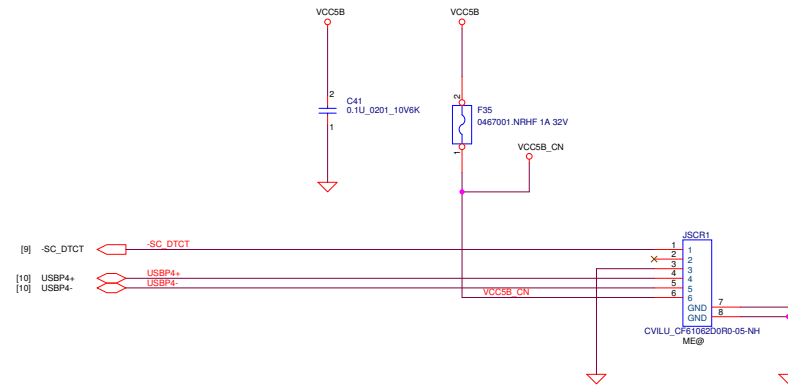


TABLE

Pin name	SD/MMC	MEMORSTICK
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7		



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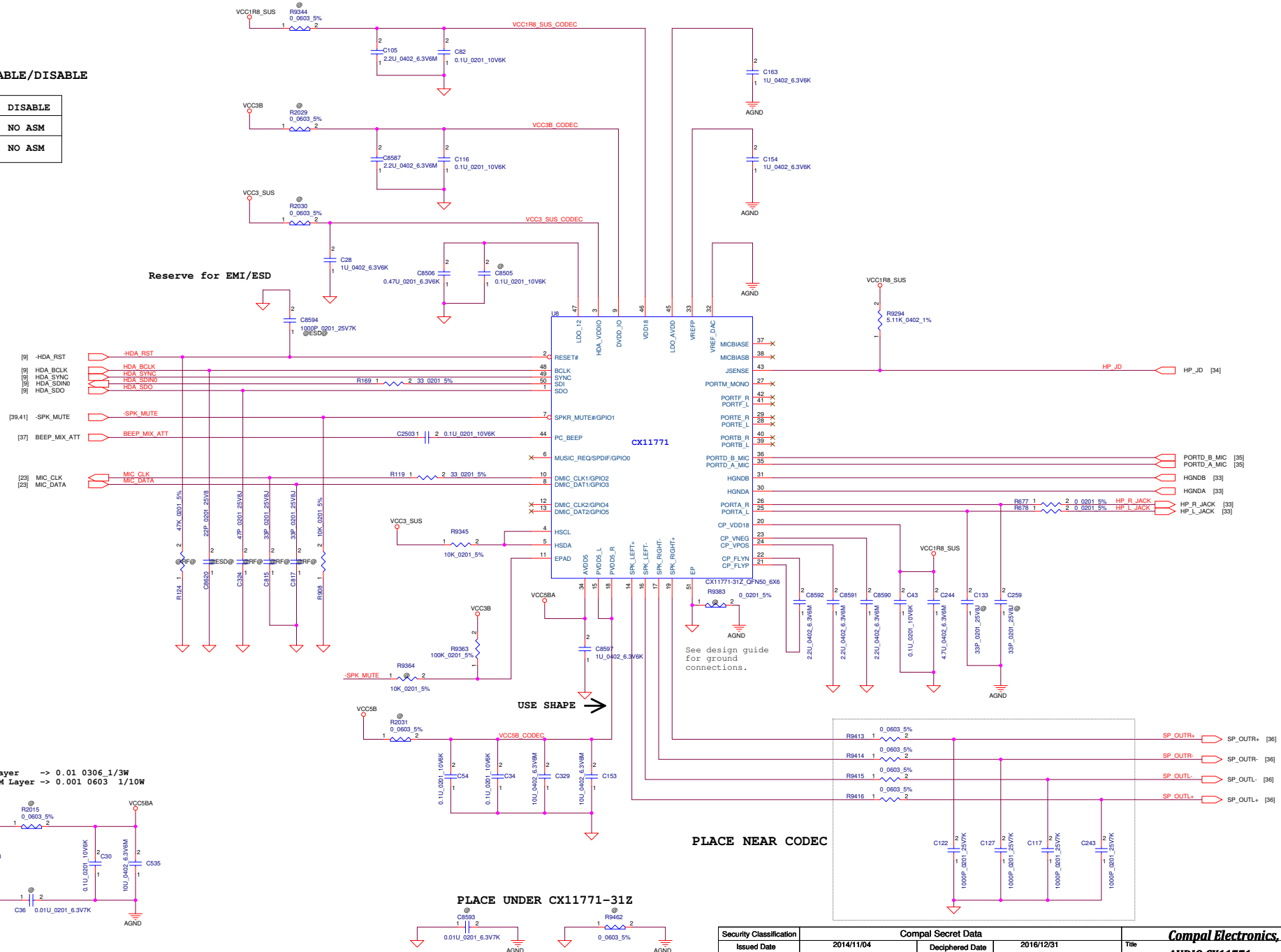


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TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R961	ASM	NO ASM
R119	ASM	NO ASM

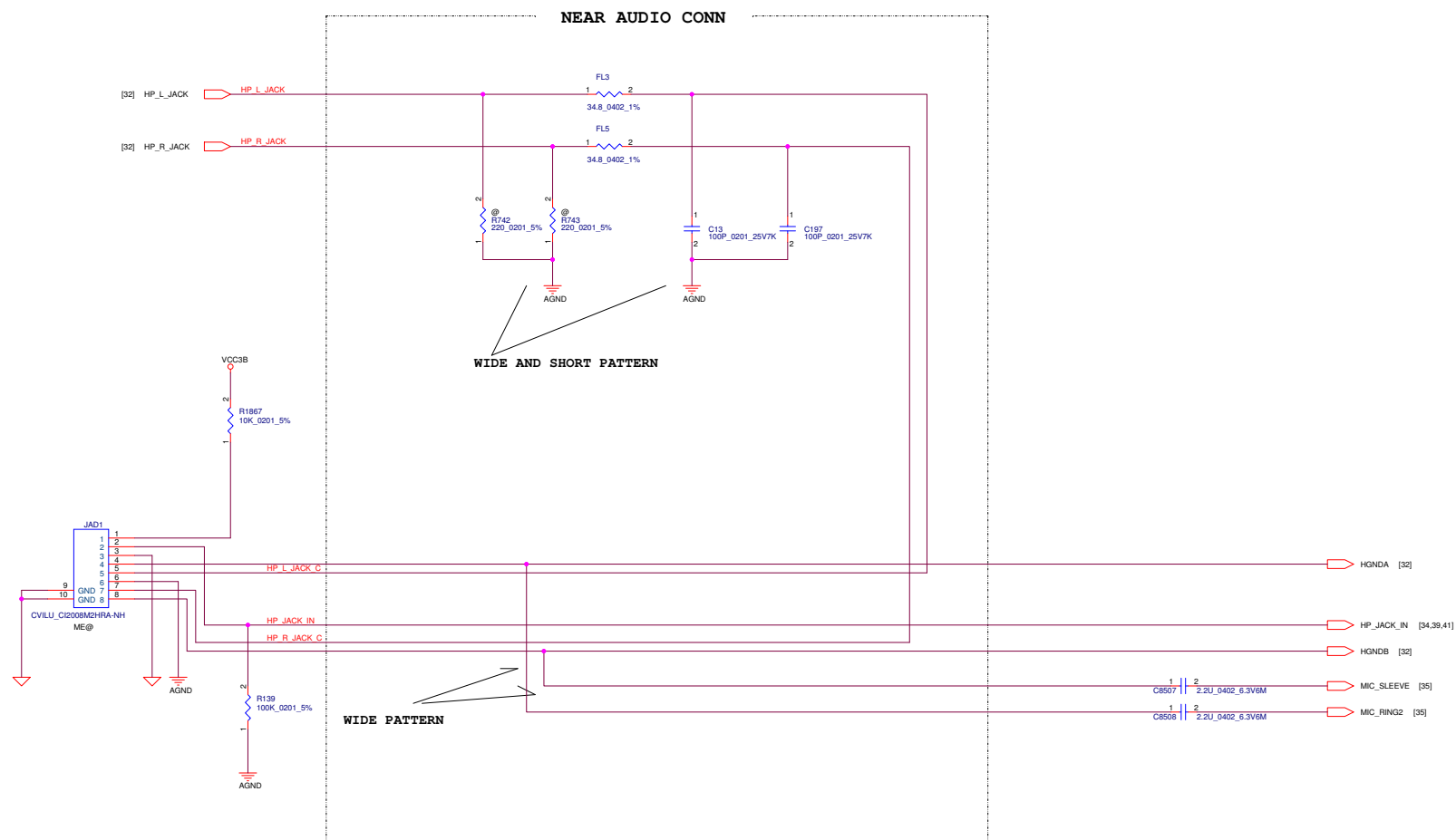
↑
LOGIC



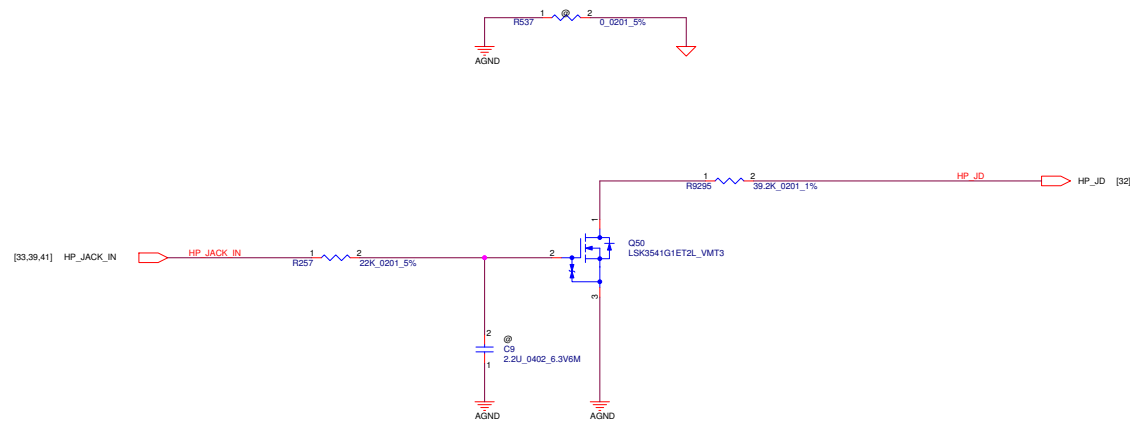
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Document Number
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Compal Electronics, Inc.
AUDIO CX11771

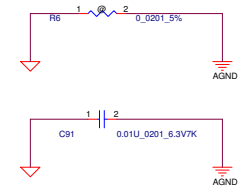
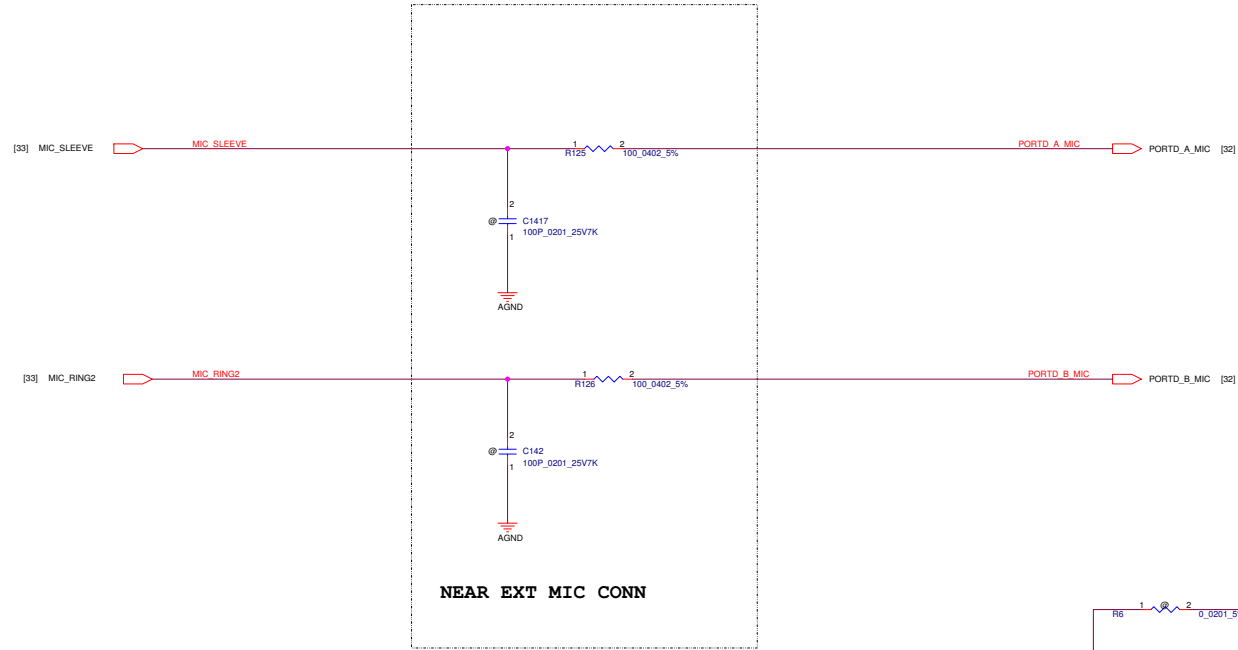
LA-E291P



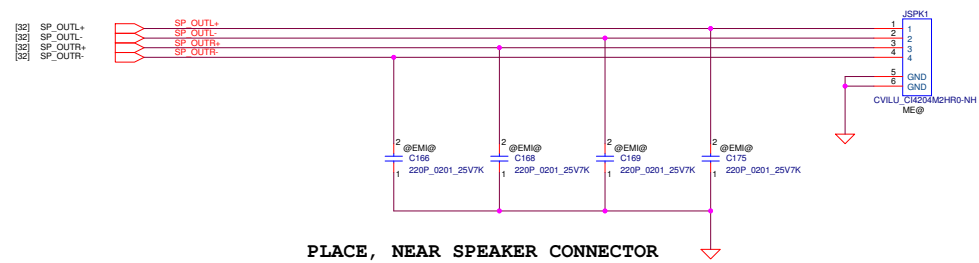
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	AUDIO CONNECTOR
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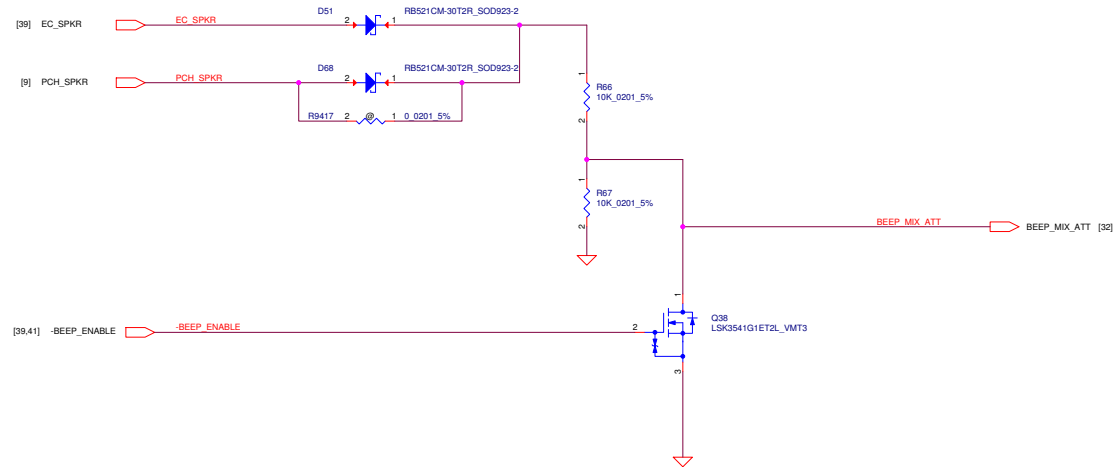
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	AUDIO JACK SENSE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-E291P
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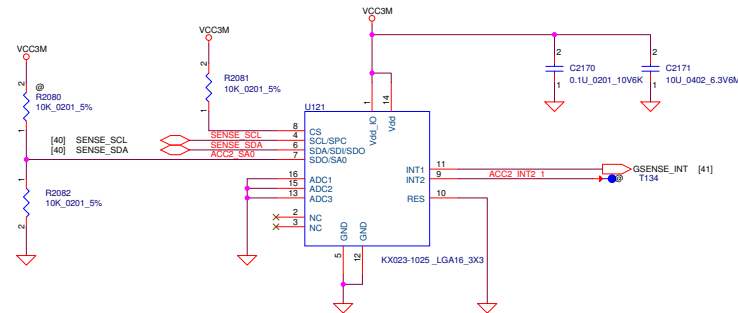
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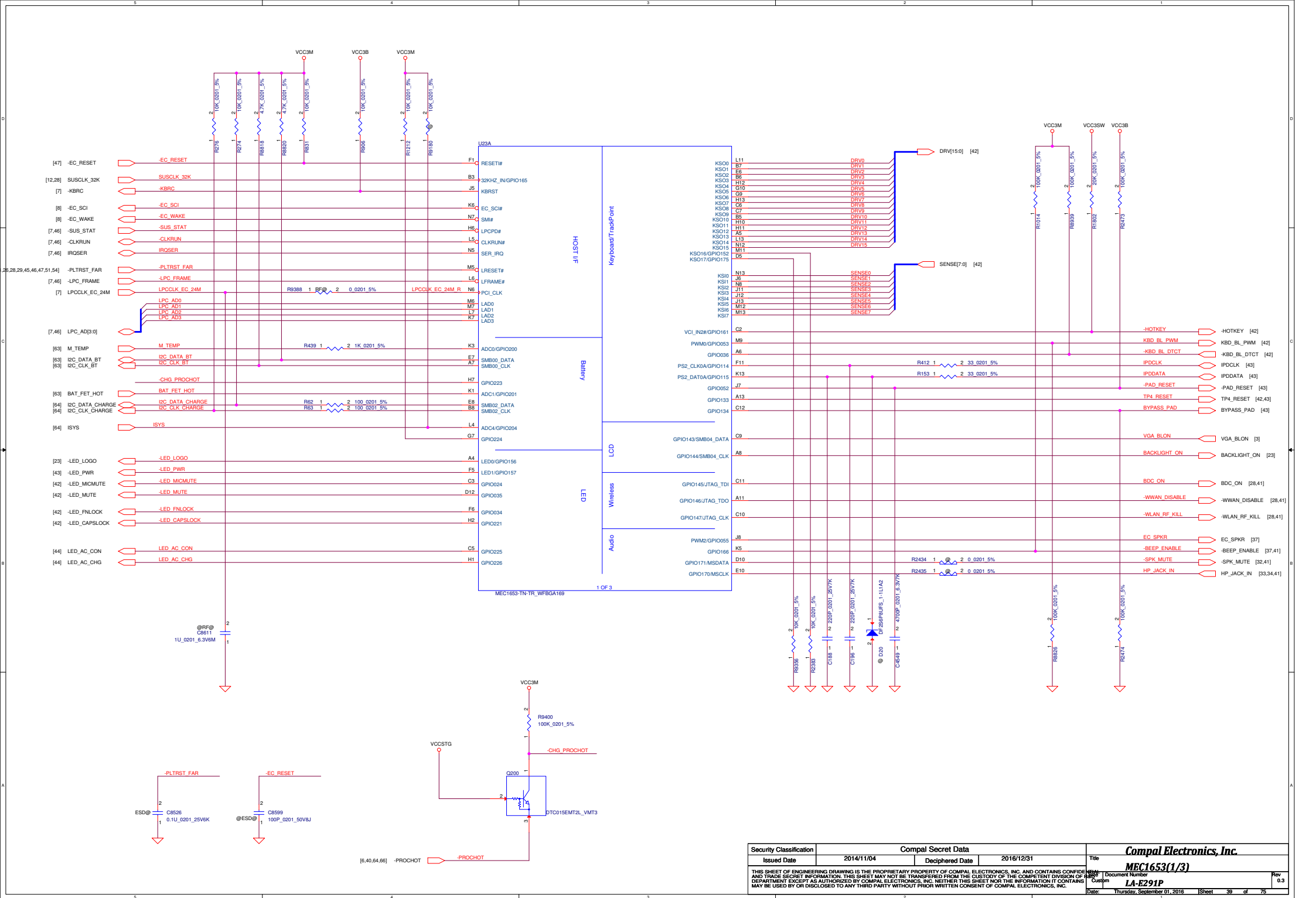
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	AUDIO BEEP
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CS	Mode Selection
H	I2C Mode
L	SPI Mode

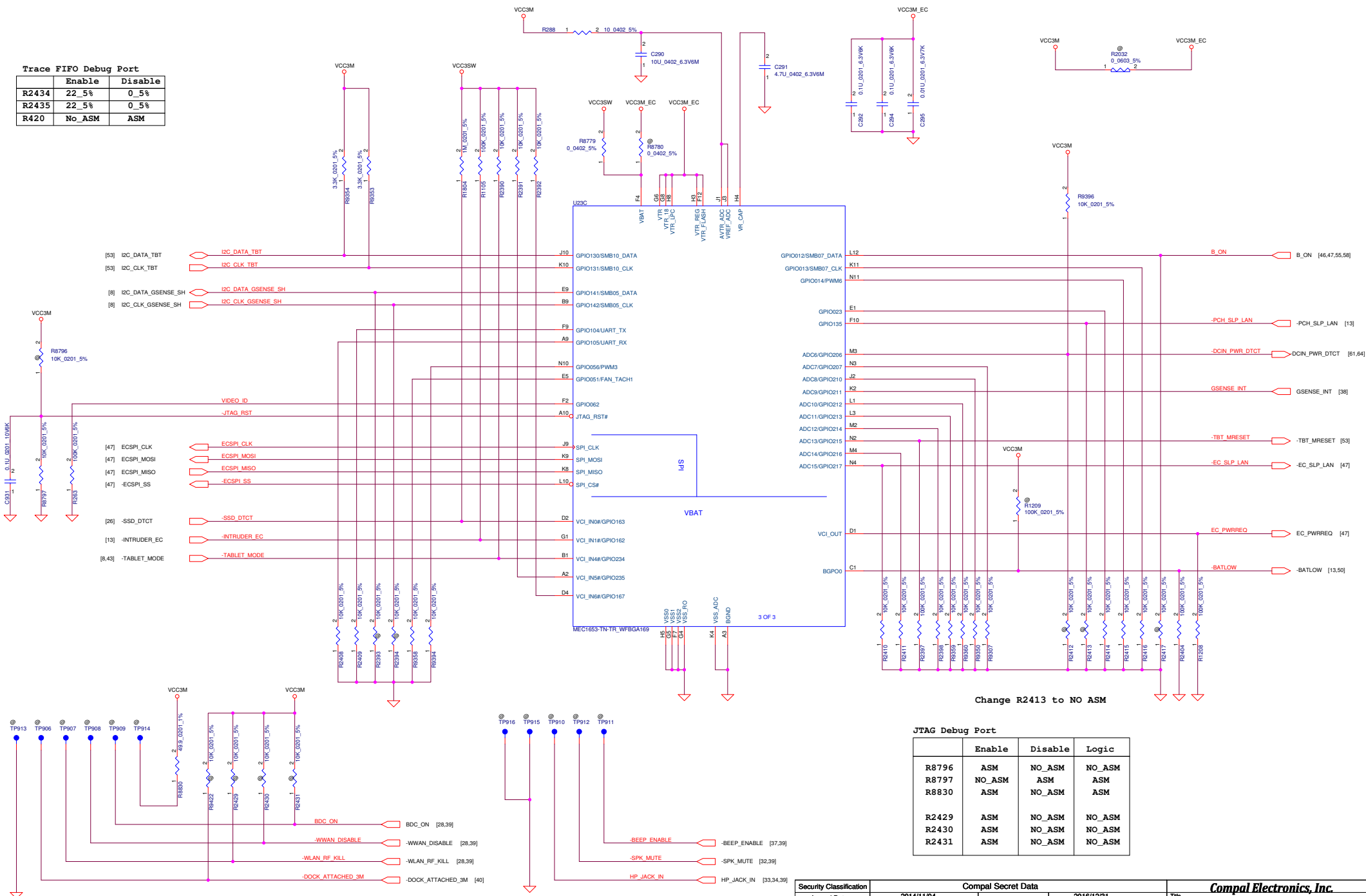
ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)

[illegible]

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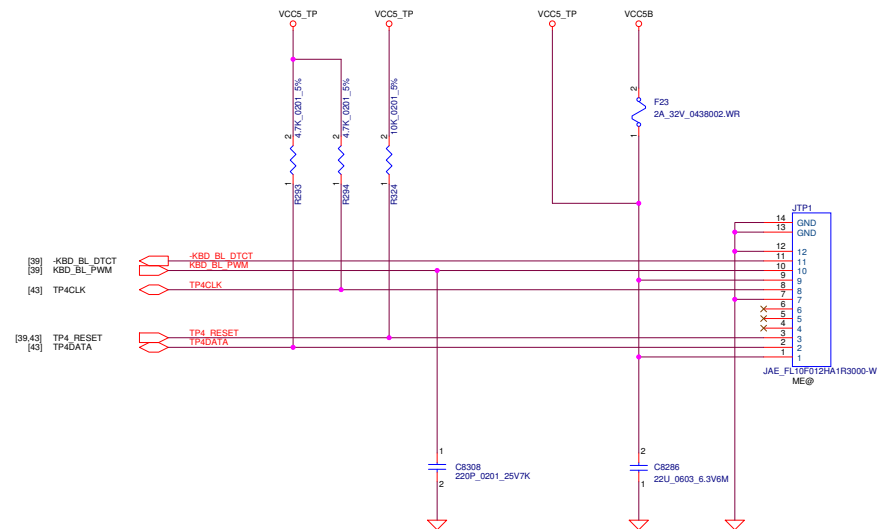
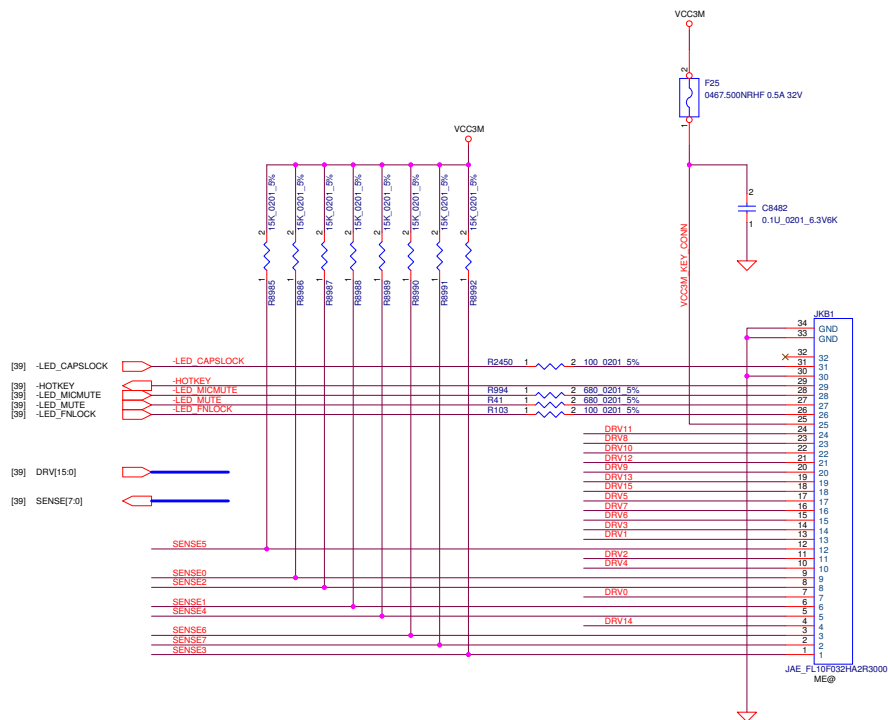


Trace FIFO Debug Port		
	Enable	Disable
R2434	22_5%	0_5%
R2435	22_5%	0_5%
R420	No_ASM	ASM



	Enable	Disable	Logic
R8796	ASM	NO_ASM	NO_ASM
R8797	NO_ASM	ASM	ASM
R8830	ASM	NO_ASM	ASM
R2429	ASM	NO_ASM	NO_ASM
R2430	ASM	NO_ASM	NO_ASM
R2431	ASM	NO_ASM	NO_ASM

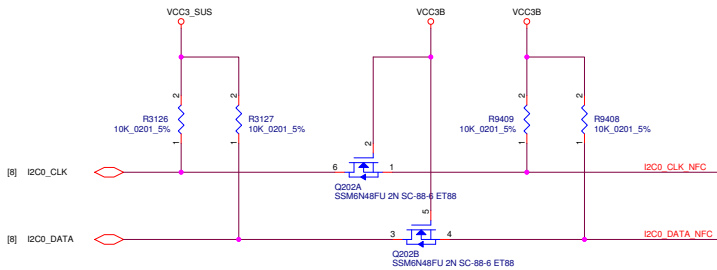
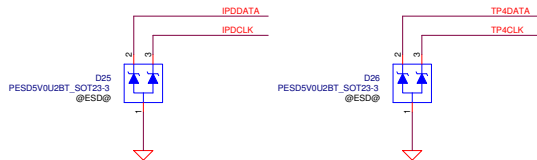
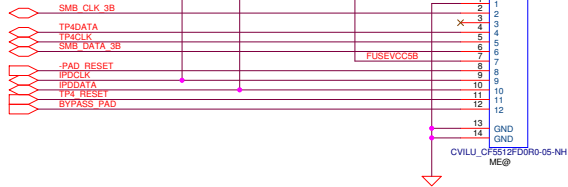
Security Classification	Compul Secret Data			Title	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	MEC1653(3/3)	
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				LA-E291P	0.3
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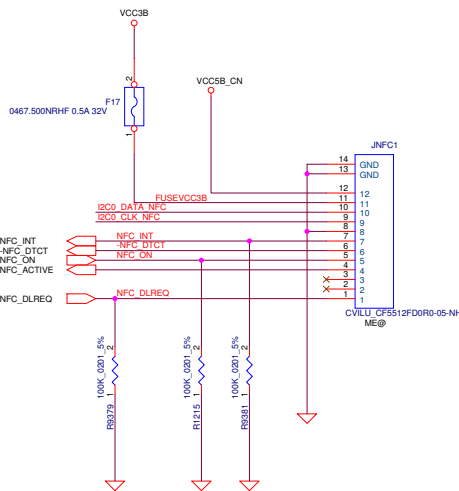
Clickpad

[21,46] SMB_CLK_3B
[42] TP4DATA
[42] TP4CLK
[21,46] SMB_DATA_3B
[39] -PAD_RESET
[39] IPDCLK
[39] IPDDATA
[39,42] TP4_RESET
[39] BYPASS_PAD

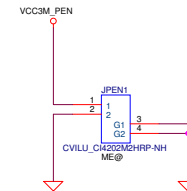
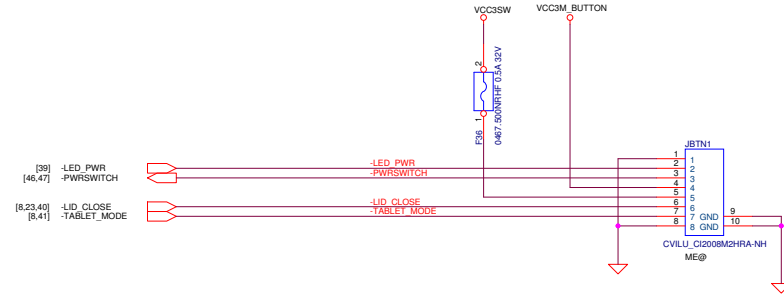
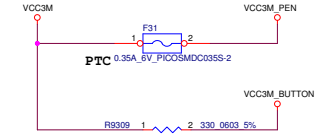


NFC

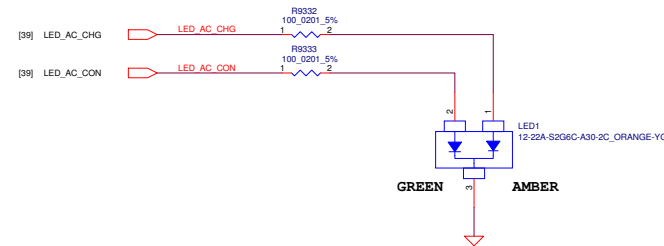
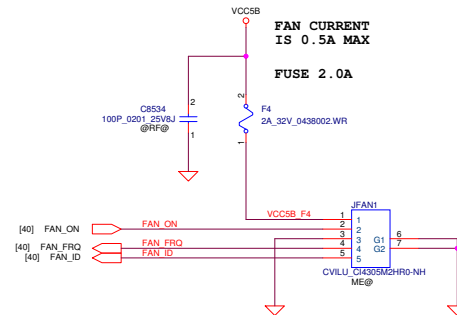
[10] NFC_INT
[8] NFC_DTCT
[10] NFC_ON
[9] NFC_ACTIVE
[8] NFC_DLREQ



TO SUB BOARD



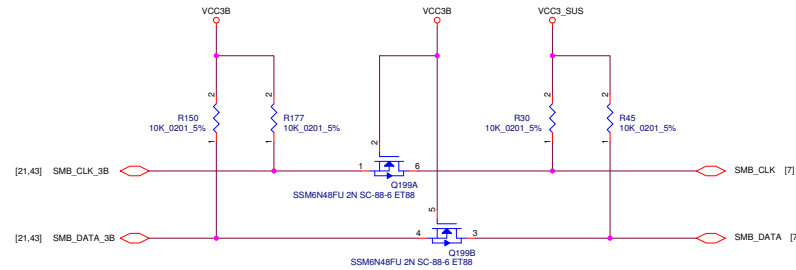
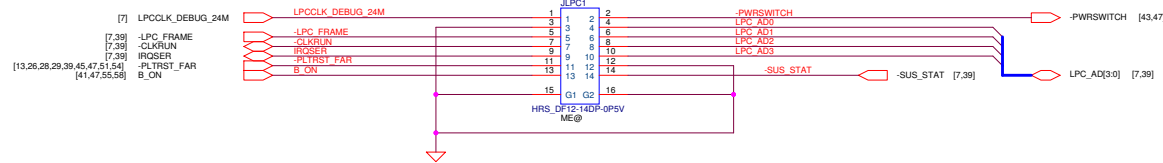
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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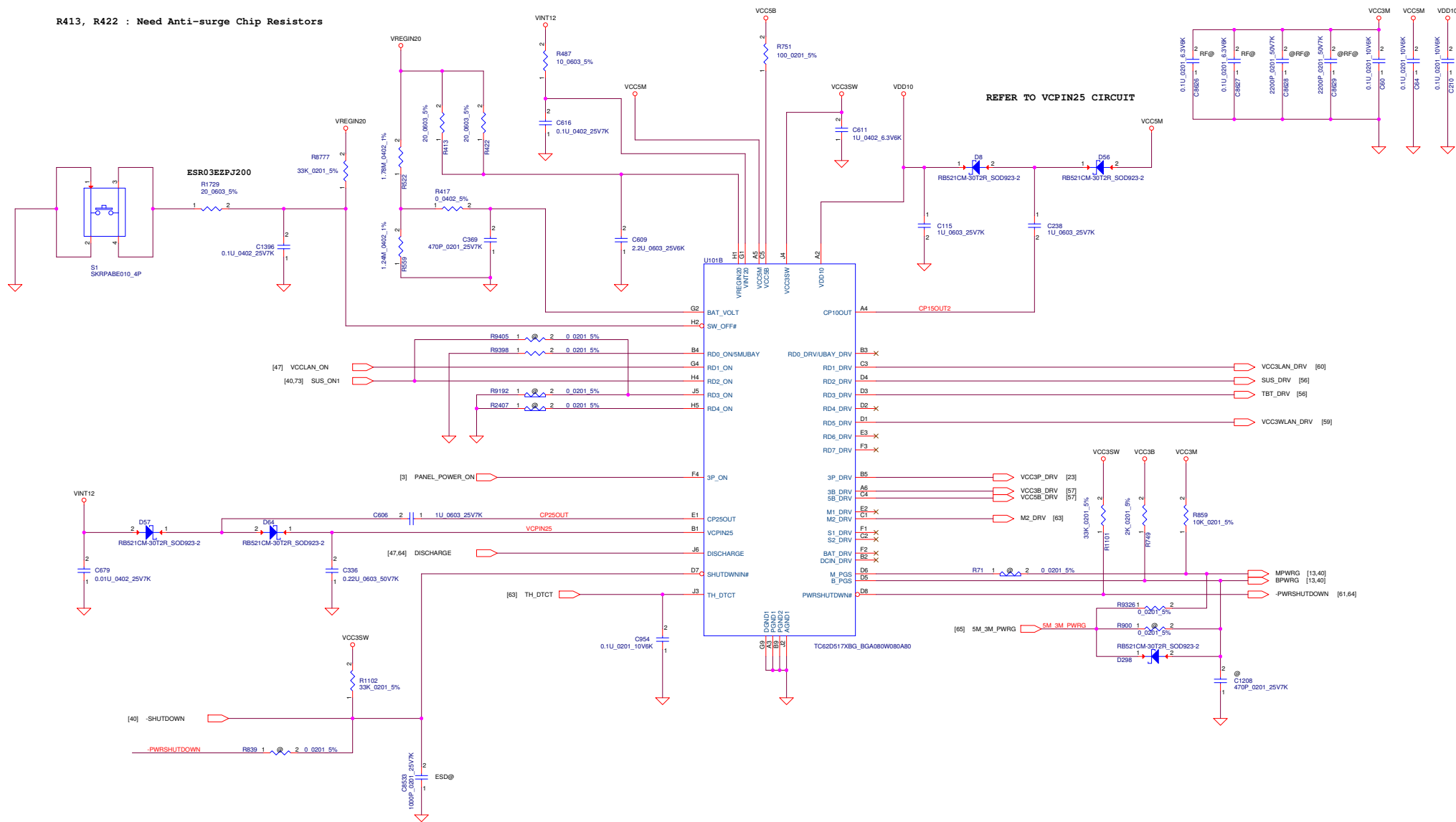
TABLE			
REF	DES	ENABLE	DISABLE
JLPC1		ASM	NO_ASM
R220		ASM	NO_ASM

↑
LOGIC



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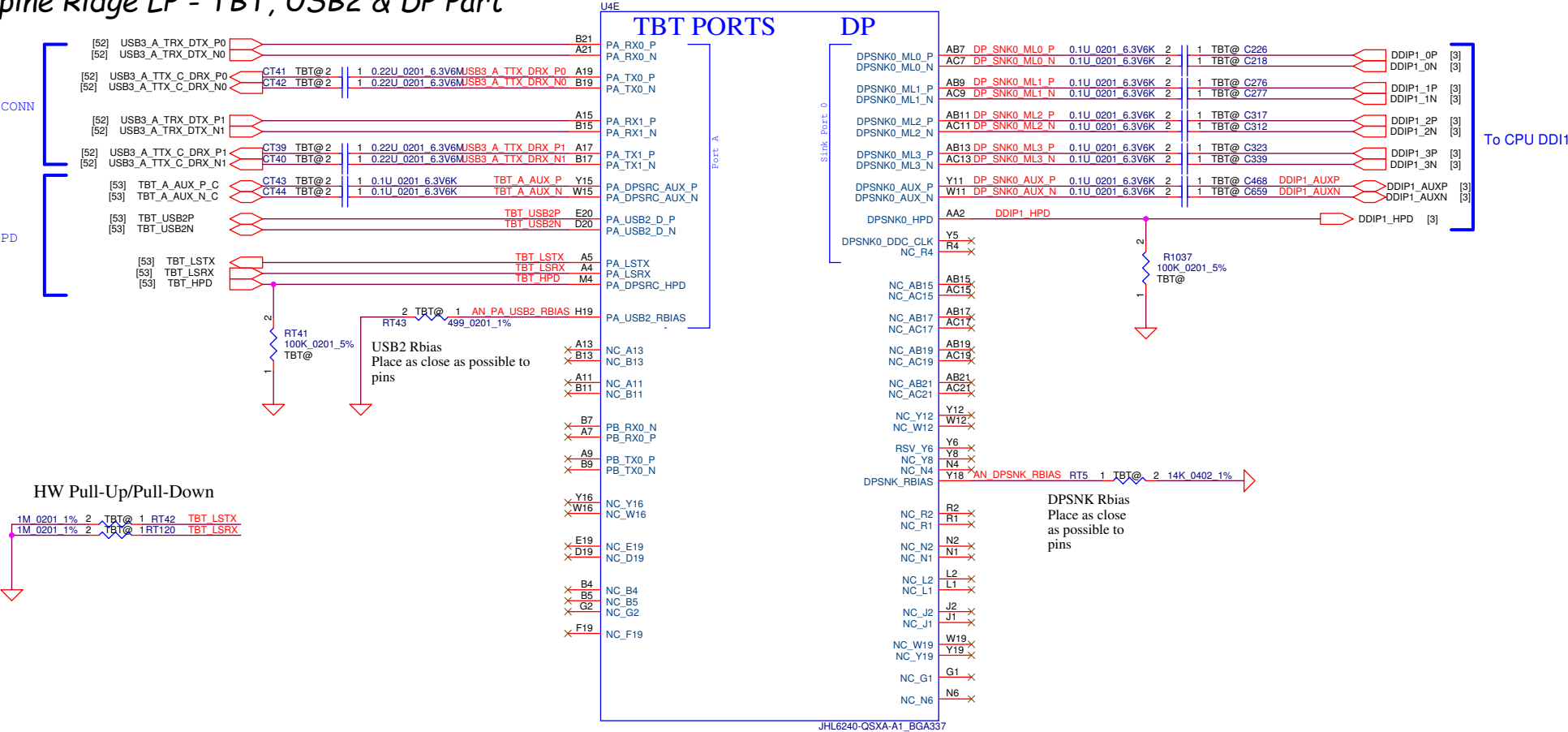
R413, R422 : Need Anti-surge Chip Resistors



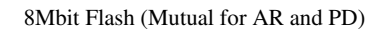
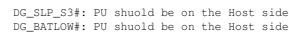
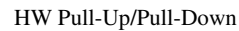
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			Date:	Thursday, September 01, 2016	Sheet 48 of 75

Alpine Ridge LP - TBT, USB2 & DP Part

Alpine Ridge LP - TBT, USB2 & DP Part



Alpine Ridge LP - Misc
Symbol

**Compal Electronics, Inc.****AR : MISC**

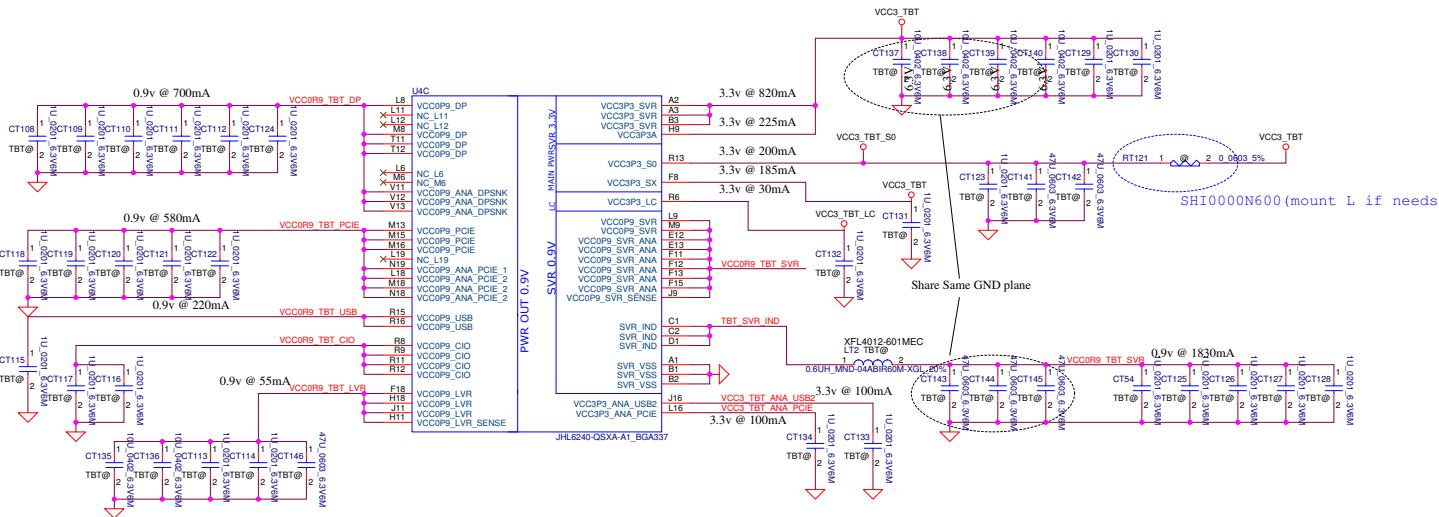
Document Number
LA-E291P

Document Number	Rev
1A-E291B	0.3

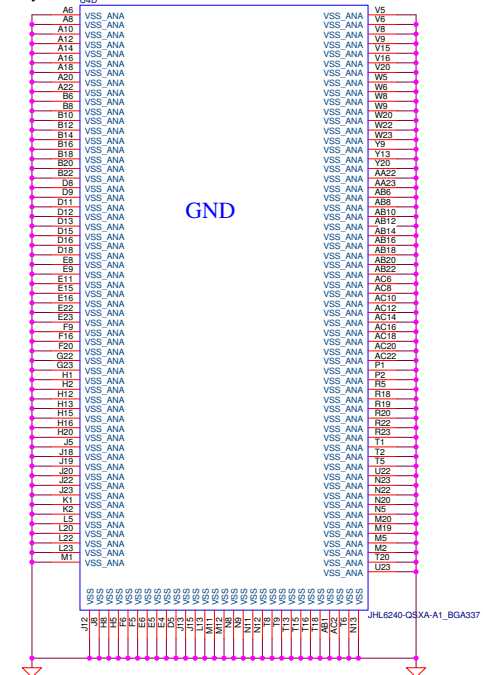
Date: Thursday, September 01, 2016		Sheet 50 of 75	
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Alpine Ridge LP - Power Supply

Alpine Ridge SP - VCC
Symbol



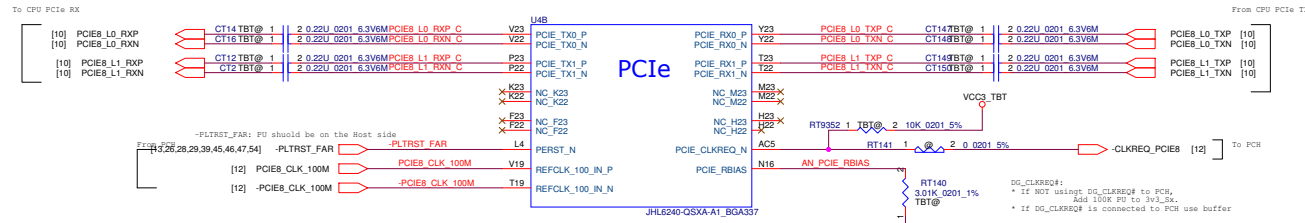
Alpine Ridge SP - GND
Symbol

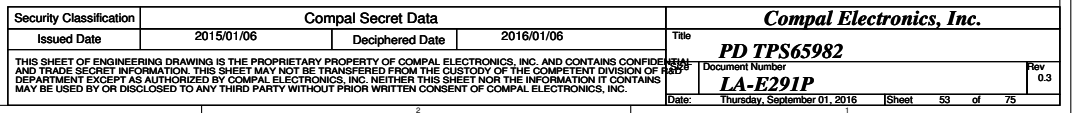


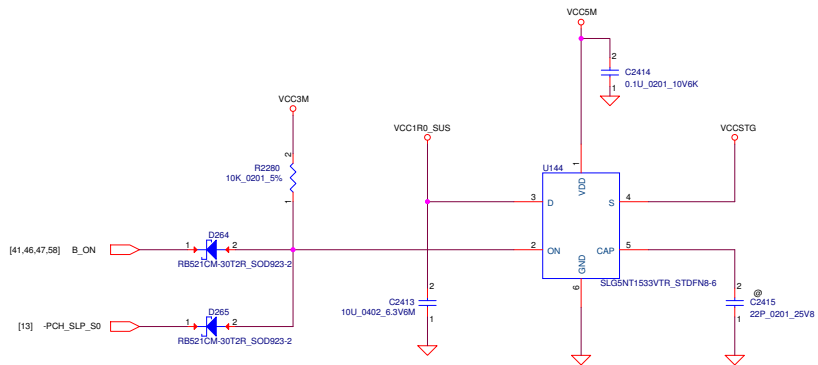
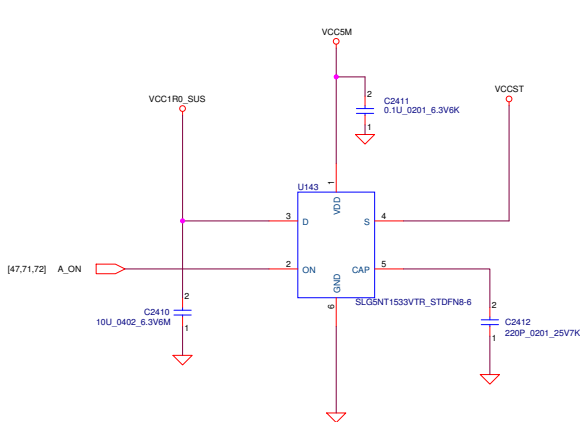
AR-LP Power & GND

AR-LP PCIE

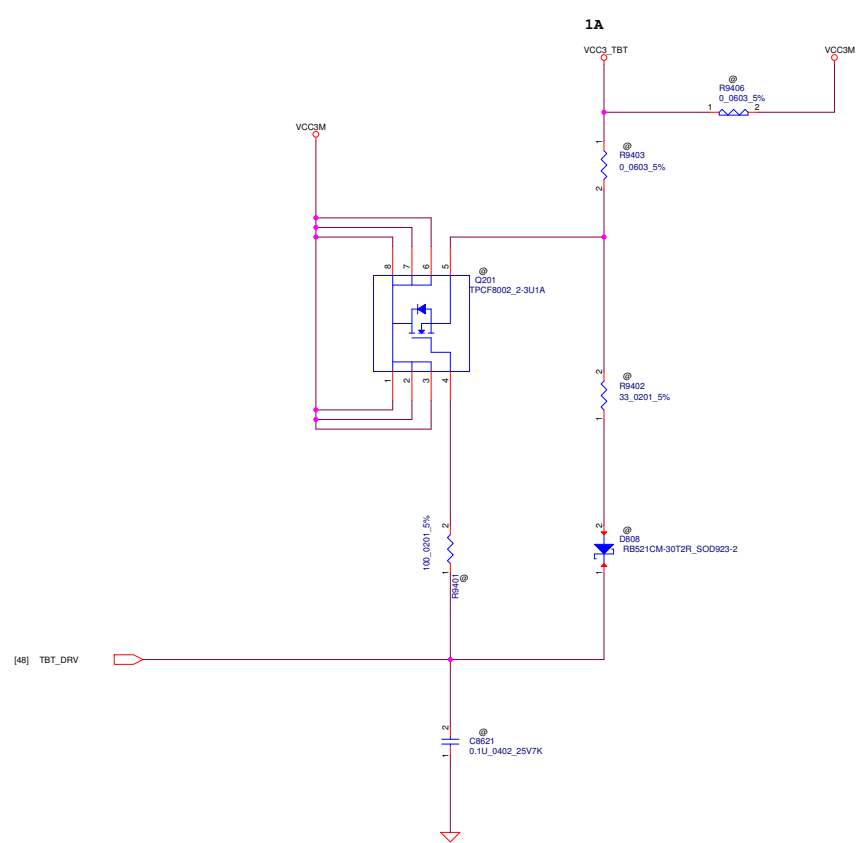
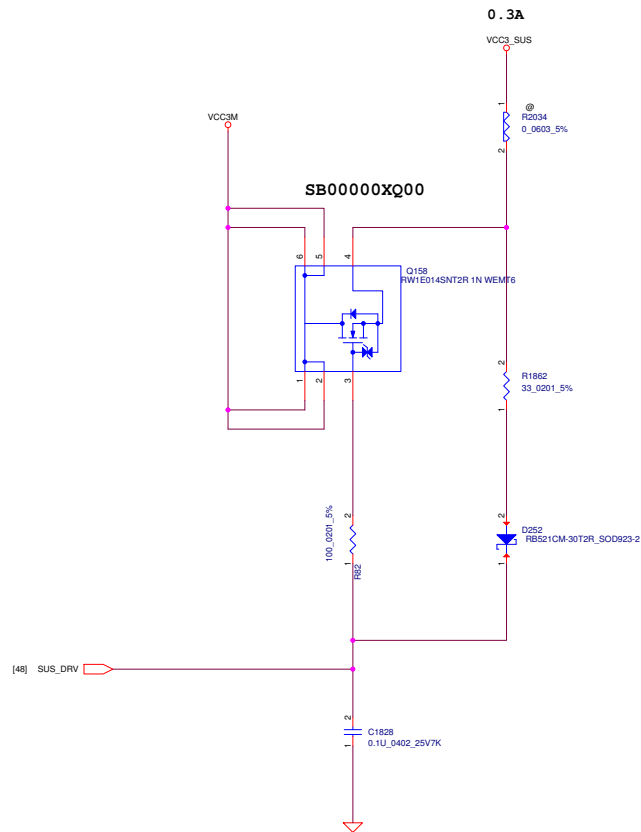
Alpine Ridge LP - PCIE
Symbol



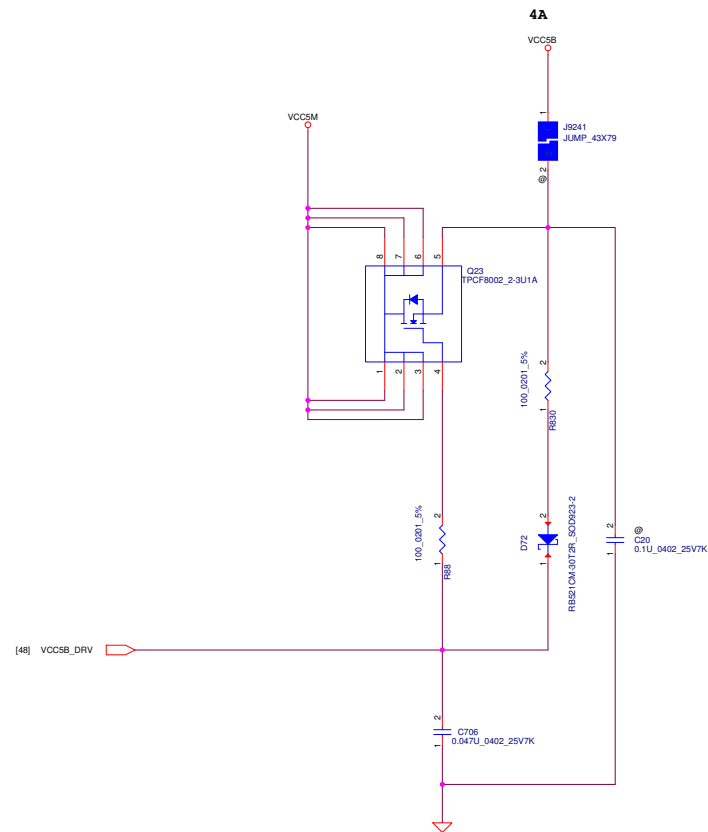
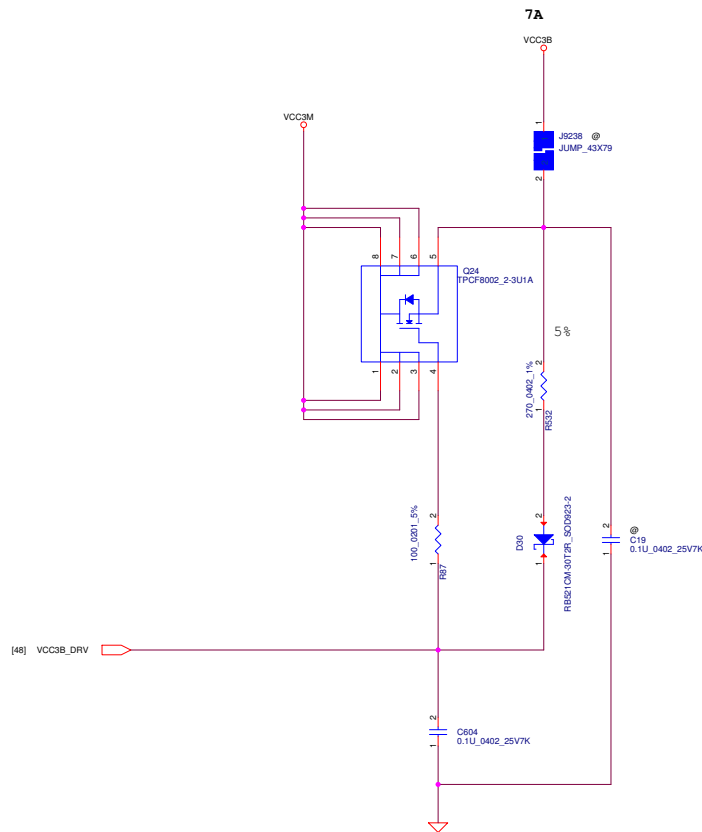




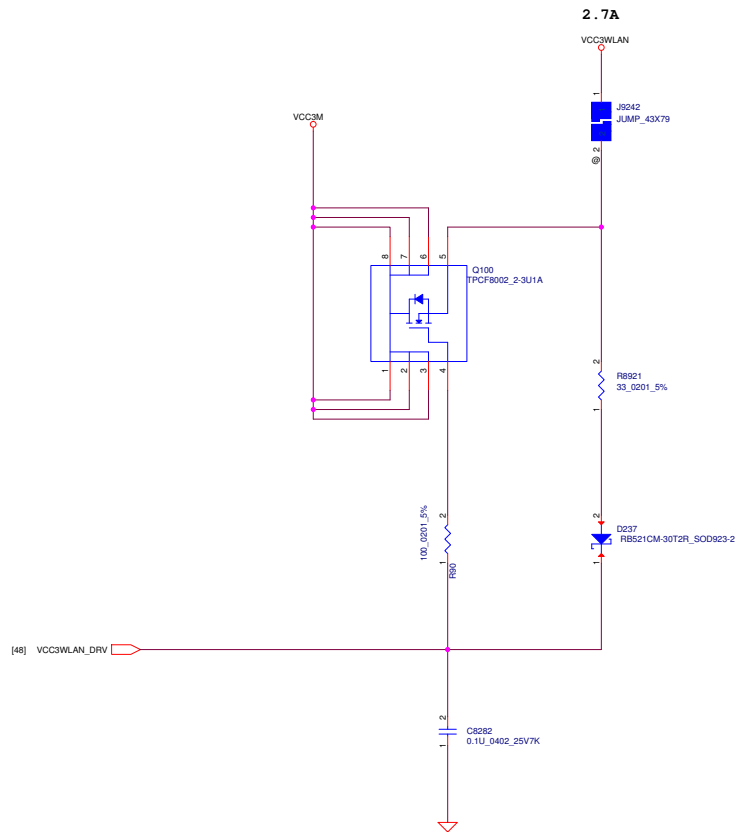
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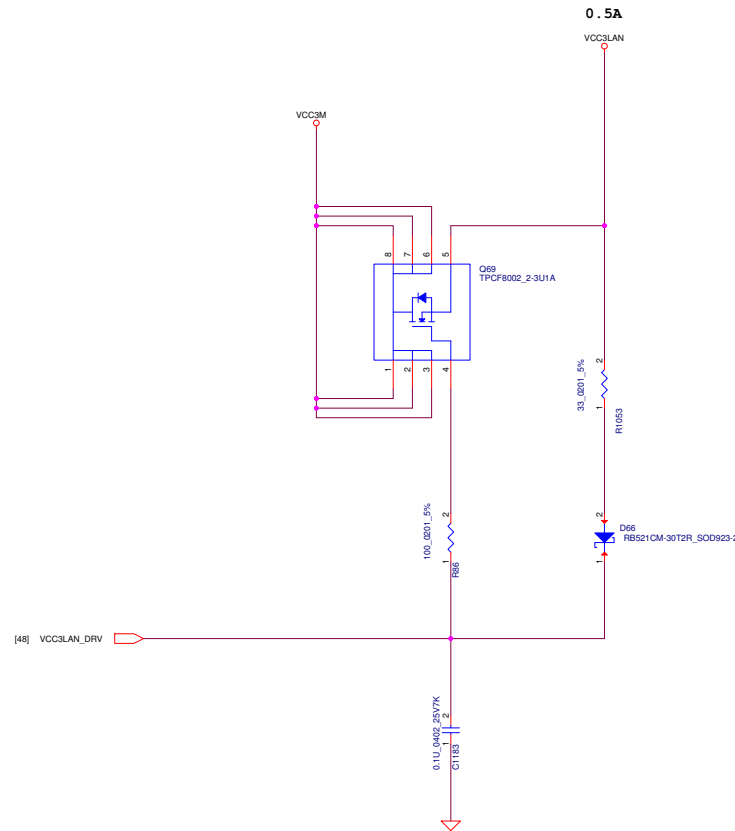
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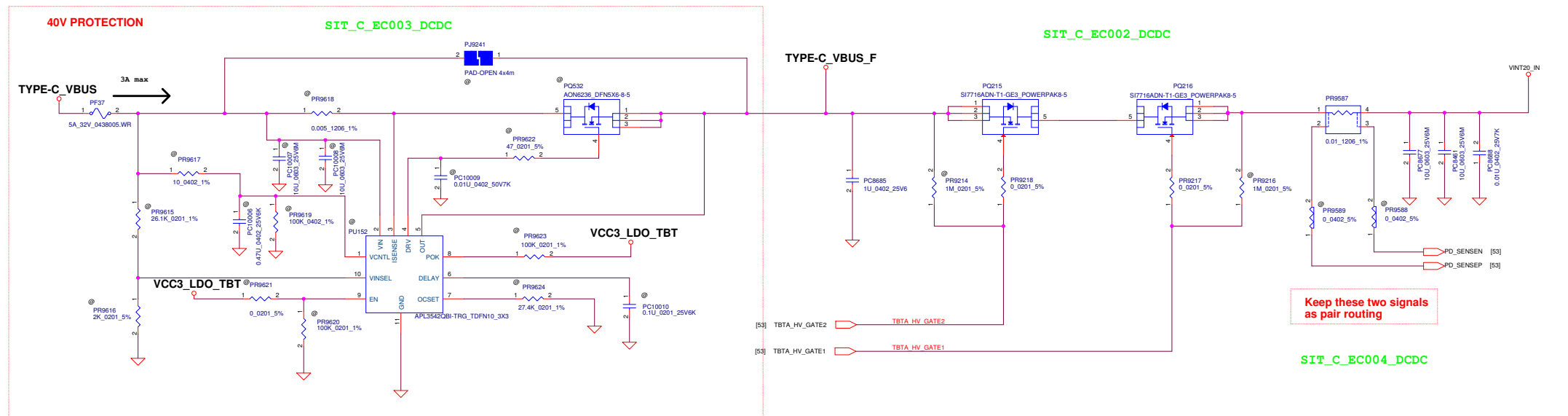
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				Date	Thursday, September 01, 2016
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	LOAD SW LAN
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MAIN BAT CONN

The schematic shows the main battery connection interface. Key components and connections include:

- Power Input:** VCC3M and M_BAT_PWR (connected to M-BAT-PWR).
- Grounding:** GND connections for the battery pack and the PCB.
- Resistors:** PR328 (6.19K_0201_1%), PR273 (100_0201_5%), PR271 (100_0201_5%), PR483 (510K_0201_5%), PR79 (100_0201_5%), and PR38 (150K_0201_5%).
- Capacitors:** PC407 (390P_0501_250V), PC198 (2200P_0501_50V), PC200 (390P_0501_250V), and PC207 (2200P_0501_50V).
- MOSFET:** P034 SI7129DNT1GE_POWERPAK1212-8-5.
- Other Components:** PF12 (10A_32V_DC12H10A-TR), I2C_CLK_BT, I2C_DATA_BT, and M_TEMP.
- Labels:** MAIN BAT CONN, WIDE PATTERN, and various component values and footprints.

[illegible]

PTC function

TH_DTCT

PR1
540_0402NEW_30%_PR115BBB41NSBRC

PR2
540_0402NEW_30%_PR115BBB41NSBRC

PR3
540_0402NEW_30%_PR115BBB41NSBRC

PR4
540_0402NEW_30%_PR115BBB41NSBRC

PR5
540_0402NEW_30%_PR115BBB41NSBRC

PR6
540_0402NEW_30%_PR115BBB41NSBRC

PR7
540_0402NEW_30%_PR115BBB41NSBRC

PR8
540_0402NEW_30%_PR115BBB41NSBRC

TABLE	Target
PR1	VCCM Switching FET Pq16
PR2	VCCM Switching FET Pq16
PR3	CHARGER SWITCHING FET Pq19
PR4	CHARGER SWITCHING FET Pq19
PR5	CHARGE NVIC MOS Pq25
PR6	BAT-PMOS2 TO B-PMOS1 Pq4
PR7	DDR Power MOS Pq12
PR8	VCCM MOSFET driver MCP1182 Pq36
PR9	VCCM MOSFET driver MCP1182 Pq36
PR10	VCCM MOSFET driver MCP1182 Pq36
PR11	DDR PMOS2 to CPU VDD Pq1
PR12	TYPE-C USB2 V MOS Pq215
PR13	CPU Gnd

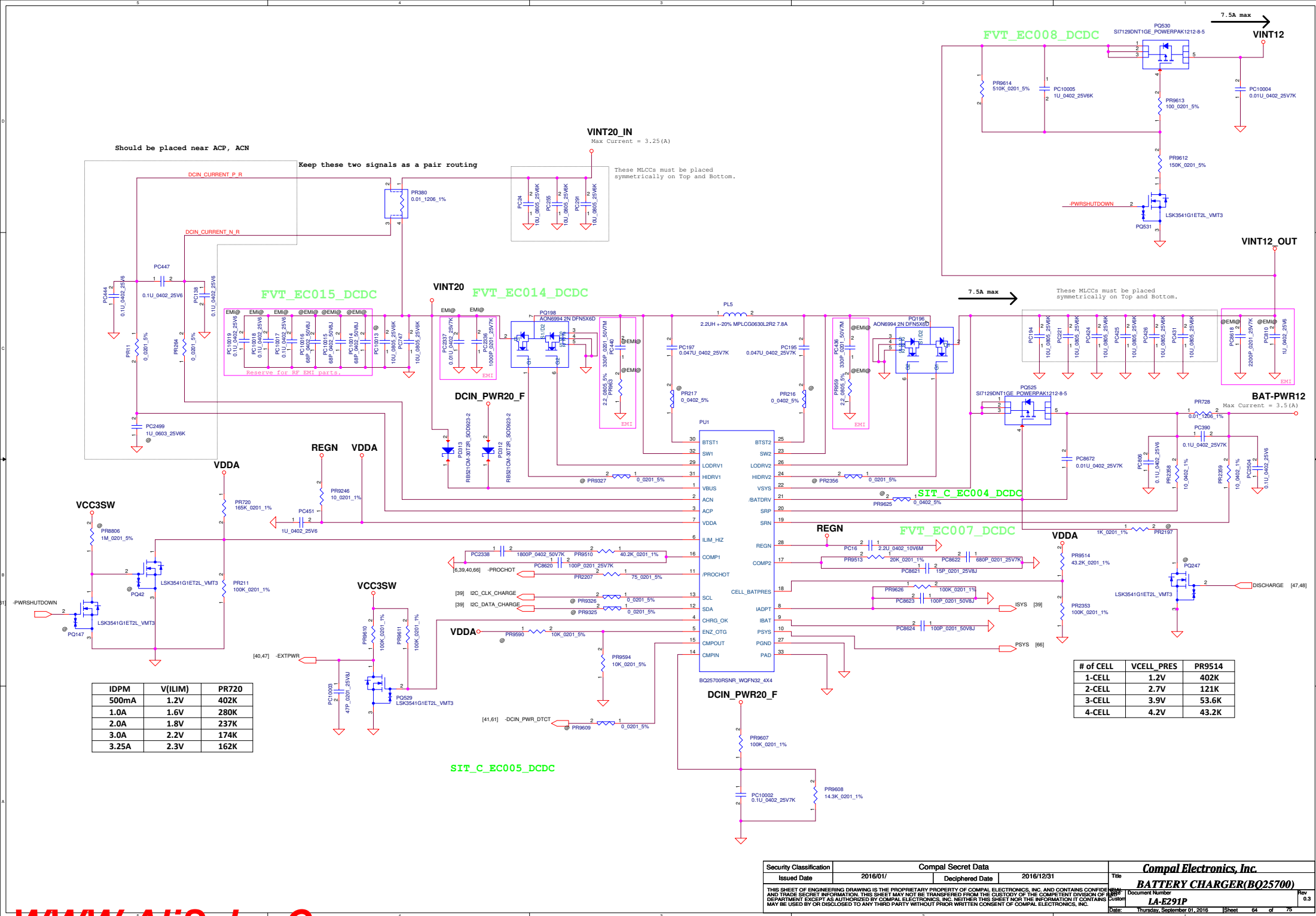
FVT_EC003_DCDC

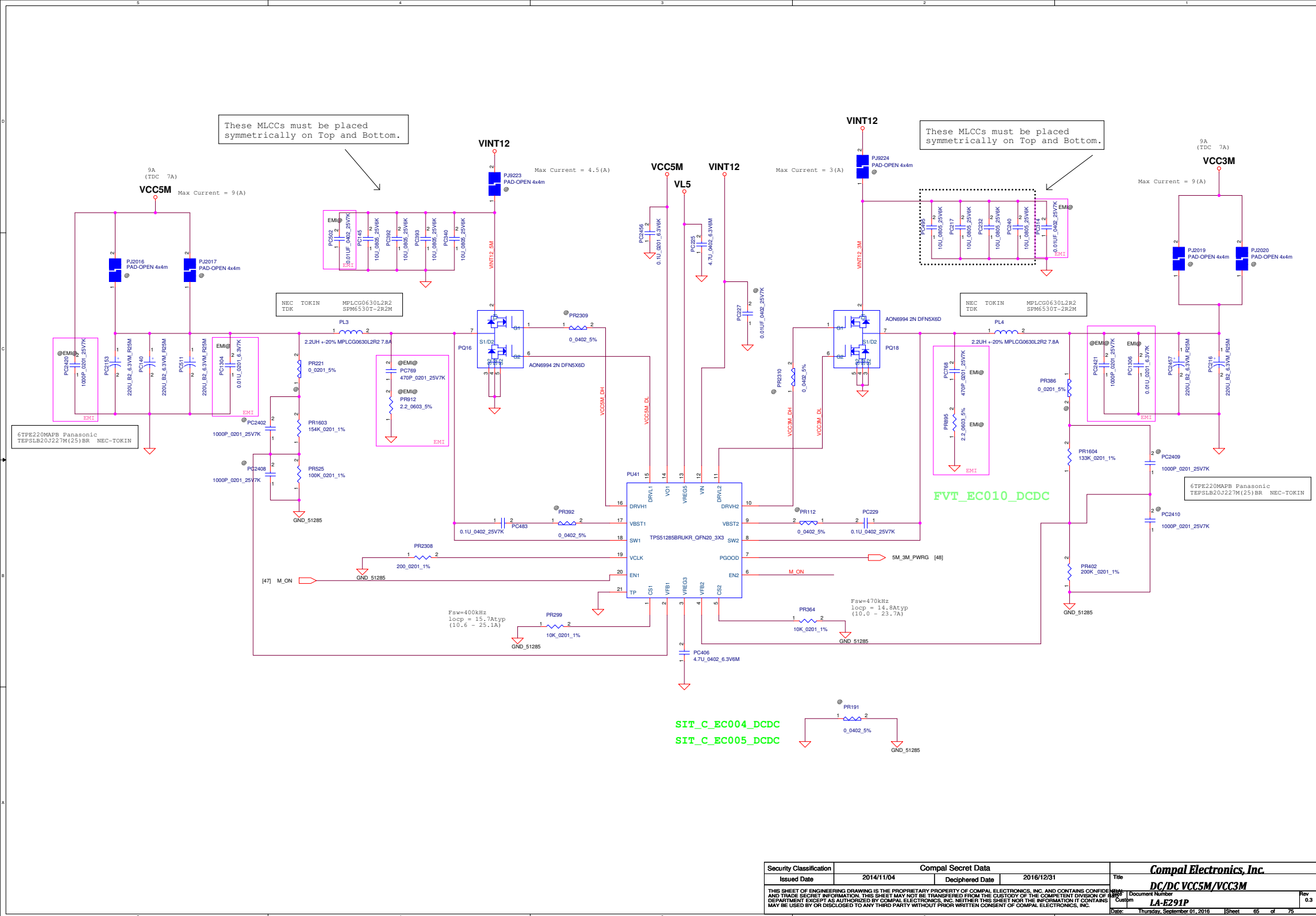
Power to ThinkEngine

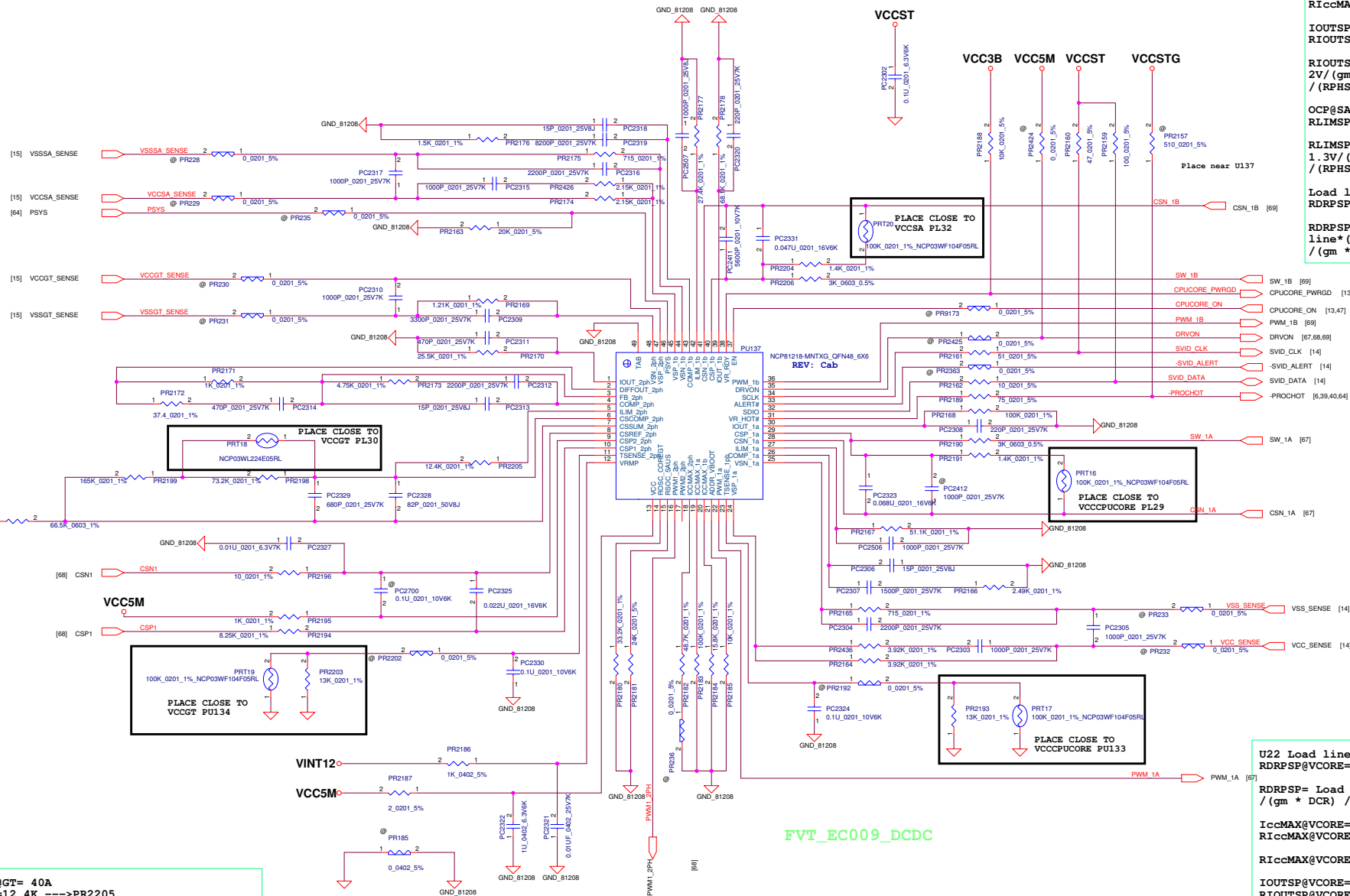
The schematic diagram illustrates the power supply for the ThinkEngine. It features a DCDC converter block that receives input from TYPE-C_VBUS and provides output to various power rails. The input side includes a 0.5A_32V_F0603FA0500V032T capacitor (PF35) and a 4.7uF_0603_25V6K capacitor (PC869). The output side includes a 0.5A_32V_F0603FA0500V032T capacitor (PF39) and a 4.7uF_0603_25V6K capacitor (PC869). The output rails are connected to the DAN222MG12L_VMD3-3 components. The diagram also shows the connection to the VREGIN20 rail.

Reserve for Type-C to ThinkEngine power.

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				Created	Thursday, September 01, 2016	
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U22 OCP@GT= 40A
 RLIM@GT=12.4K ---->PR2205
 RLIM= IoutLIMIT * Load line/10

U22 IccMAX@GT= 31A
 RIccMAX2ph= 48.7K ---->PR2182
 RIccMAX2ph= (IccMAX2ph+32)*200K Ohn/ 127

U22 Iout@GT= 31A
 RIOUT@GT=25.5K ---->PR2170

RIOUT= 2* RLIM / (10 *IOUTICMAX * Load line)

U22 Load line@GT= 3.1m
 RPH@GT=84.5K ---->PR130,PR138

Load line= (RCS2+(RCS1*Rth)/(RCS1+Rth))
 *IOUTTOTAL * DCR/RPH

TABLE OCP

PR2167	51.1K	Ilim=40A	VCCCPUCORE
PR2205	12.4K	Ilim=40A	VCCGFXCORE
PR2177	27.4K	Ilim=10A	VCCSA

SIT_C_EC004_DCDC

SIT_C_EC005_DCDC

FVT_EC009_DCDC

RIccMAX@SA= 5A
 RIccMAX@SA= 15.8K ---->PR2184

RIOUTSP@SA= 5A
 RIOUTSP@SA=84.5K ---->PR2178

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR / (RPHSP+Rth+RCSSP))

OCP@SA= 10A
 RLIMSP@SA=27.4K ---->PR2177

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR / (RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
 RDRPSP@SA=2.15K ---->PR2174

RDRPSP= Load line*(RPHSP+Rth+RCSSP) / (gm * DCR) / (Rth+RCSSP)

U22 Load line@VCORE= 2.35m
 RDRPSP@VCORE=3.92K ---->PR2436

RDRPSP= Load line*(RPHSP+Rth+RCSSP) / (gm * DCR) / (Rth+RCSSP)

IccMAX@VCORE= 32A
 RIccMAX@VCORE= 100K ---->PR2183

RIccMAX@VCORE= IccMAX*2V/10uA/64A

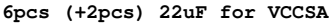
IOUTSP@VCORE= 32A
 RIOUTSP@VCORE=100K ---->PR2168

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR / (RPHSP+Rth+RCSSP))

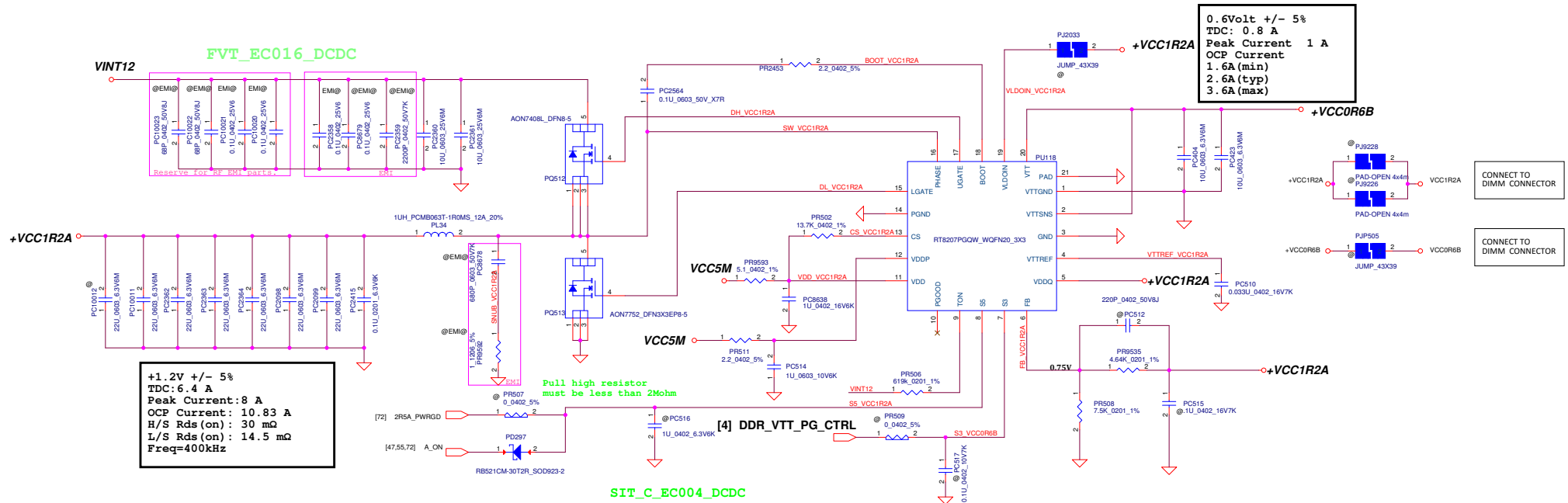
OCP@VCORE= 40A
 RLIMSP@VCORE=51.1K ---->PR2167

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR / (RPHSP+Rth+RCSSP))

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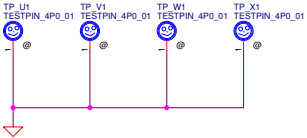
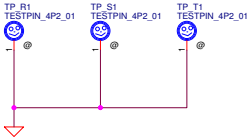
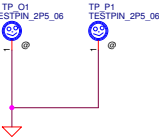
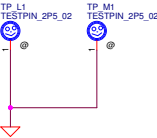
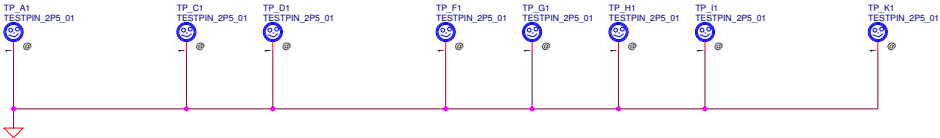


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PTH FOR SCREW HOLE

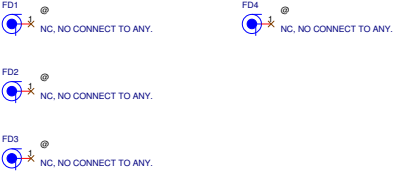
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		TOP	BOTTOM	
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TESTPIN_2P5_02	2.5	7.4	7.4	2
TESTPIN_2P5_03	2.5	Square	0	1
TESTPIN_2P5_06	2.5	5	5	2
TESTPIN_2P8_01	2.8	0	Square	1
TESTPIN_4P3_01	4.3	6.5	6.5	3
TESTPIN_4P0_01	4.0	6.1	6.1	4



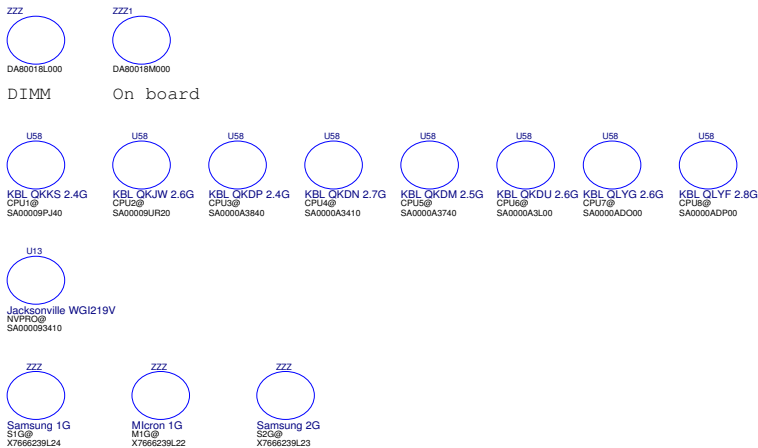
TP_Y1
H_2P5N
H_2P5N

TP_E1
H_4P0X2P5N
H_4P0X2P5N

FID
Board Area



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BOM Structure Table

BTO Item	BOM Structure	Remark
vPRO LAN chip	VPRO@	WGI219LM
non vPRO LAN chip	NVPRO@	WGI219V
Thunderbolt requirement	TBT@	
Thunderbolt reserve	@TBT@	
ESD requirement	ESD@	
ESD reserve	@ESD@	
EMI requirement	EMI@	
EMI reserve	@EMI@	
RF requirement	RF@	
RF reserve	@RF@	
XDP	XDP@	
On board RAM	X76@	